Honeywell

Process Management
Systems Division

MODEL AFDD
FLOPPY DISC DRIVE UNIT
Hardware Maintenance Manual

PE-13-100
3/83

MODEL AFDD FLOPPY DISC DRIVE UNIT HARDWARE MAINTENANCE MANUAL

The following notice is provided in accordance with the United States Federal Communications Commissions (FCC) regulations.

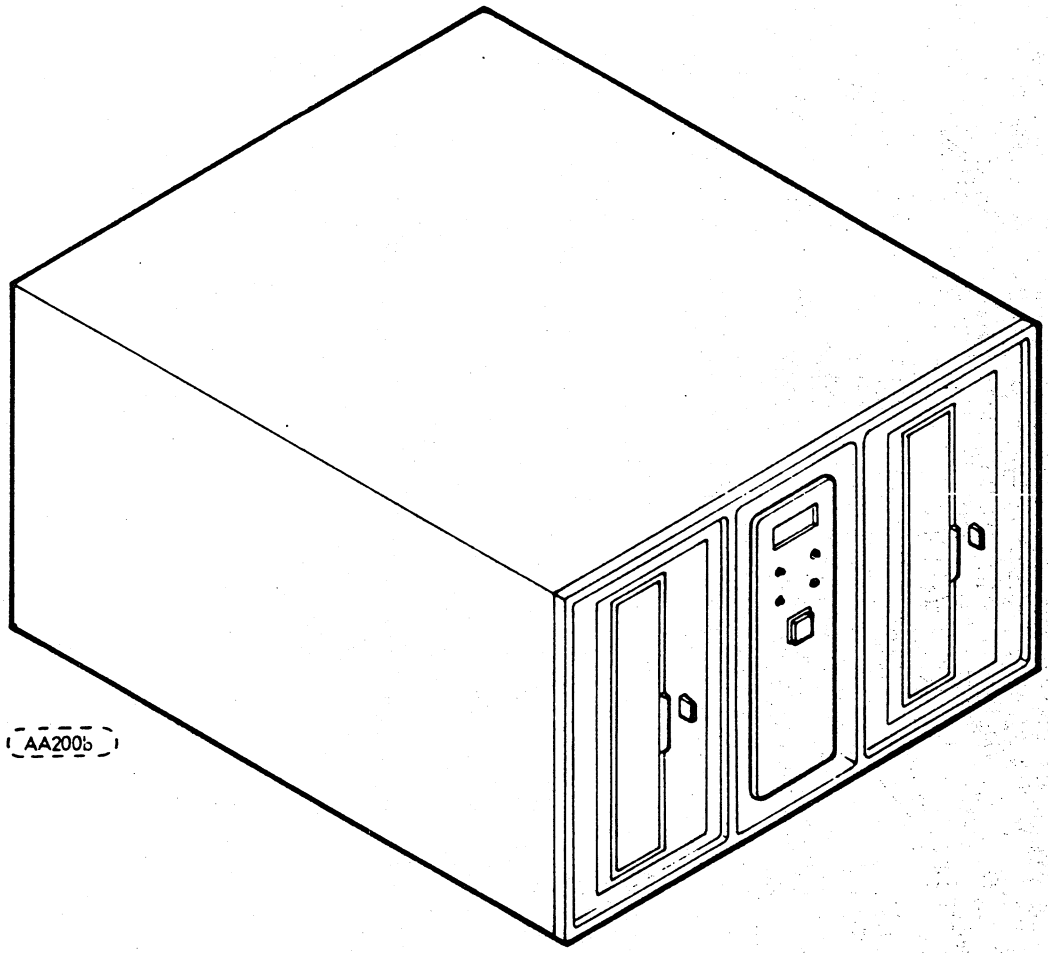
WARNING

This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with limits for Class A computing devices persuant to Subpart J of Part 15 of FCC Rules, which are designed to proivde reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES



FDDS (Master or Slave)

1 GENERAL DESCRIPTION

1.1 GENERAL

This manual describes the Honeywell Model AFDD Floppy Disc Drive Unit. In this manual, the AFDD is referred to as the Flexible Disk Drive Subsystem (FDDS). Honeywell TDC 2000 Systems use the FDDS with the 9404 single sided Flexible (Floppy) Disk Drive (FDD).

1.2 APPLICABLE DOCUMENTS

DOCUMENT NO.	TITLE
PE-13-110	Floppy Disc Drive Hardware Maintenance Manual
AFDS-T	Floppy Disc Subsystem Theory
AFDS-M	Floppy Disc Subsystem Maintenance
AFDS-S	Floppy Disc Subsystem Technical Data and specification

1.3 GENERAL DESCRIPTION

The Honeywell Flexible Disk Drive Subsystem provides random-access, cost-effective peripheral data storage to a wide variety of data processing, communications or other applications.

The host system interface utilizes a 9475 Controller Adapter using industry-standard TTL single-ended transmitters and receivers for ease of overall system integration. Standard software commands between the 9475 and the host system identify information at the interface as data, function, track address, or sector address. Additional lines synchronize data transfers, provide interrupt signals, and monitor drive operation.

Using microcoded commands resident in a read-only memory (ROM), the 9474's microprocessor controller accomplishes track selection, head loading, IBM 3740 single-density or CDC Double-Density format recognition and/or generation, data transfer, error detection, status reporting and other tasks with a minimum of software support.

The 9474 Flexible Disk Drive Subsystem is available with up to four 9404 single-sided Flexible Disk Drives for a maximum capacity of 3.2 megabytes or up to four 9406 two-sided Flexible Disk Drives for a maximum capacity of 6.4 megabytes.

Any mix of single sided or two sided drives up to a total of 4 drives may be accommodated. Single and double density diskettes can be mixed. If the 9406 is used both single and two sided diskettes may be accommodated.

The 9474 FDDS incorporates a universal power supply. A range of voltage sources from 100 to 250 VAC at either 50 or 60 Hz can be used providing coverage of both domestic and foreign markets without the inconvenience of engineering special power-supply adaptions.

1.4 MAJOR COMPONENTS

The following parts are major components which comprise the FDDS.

1.4.1 MECHANICAL FRAMEWORK

The FDDS mechanical framework and packaging provide basic construction for either desk top or rack mounting for the integration and operation of unit components. The Master unit provides for the mounting of: two FDD units; controller adapter (FDA); power supply, system cabling and I/O connector; additional printed circuit card spare for customer oriented interface; air distribution system; and AC power controls. Identical in appearance to the control cabinet, the Slave unit provides a second cabinet, in either desk top or rack mount for mounting of: two additional FDD units; power supply system cabling and I/O connector; air distribution system; and AC power controls (see Figure 1-1). In this manual the unit containing the controller adapter is called the Master and the second unit is called the Slave.

1.4.2 FDD UNIT

The FDD is a low cost random access storage device utilizing a single removable disk cartridge as the storage medium. The disk itself is 7.88 inches (20.1 mm) in diameter and is contained in an 8 inch (20.3 mm) square protective envelope. To load the disk, the entire envelope is inserted into a slot in the FDD behind a small access cover.

Rotating at 360 r/min, data is read or written on any one of the 77 tracks of one of the recording surfaces at a rate of 249,984 bits per second (single density) or 499,968 bits per second (double density) to provide a total unformatted capacity of 3.21 or 6.42 megabytes. The unformatted capacity for the two-sided FDD is 6.42 megabytes for single density and 12.8 megabytes for double density recording. The single head or double head assembly need only be in contact with the media during actual data transfer operations. Track accessing is accomplished using a stepping motor. Index is detected using a photo-optical technique to sense the physical index hole in the disk cartridge.

The FDD contains all the analog read, write and control electronics necessary to perform data transfer operations using only simple control commands and provides write protect capability. For additional detailed information on the FDD refer to the CDC Flexible Disk Drive Manual given on the preface page.

1.4.3 FDDS CONTROLLER ADAPTER (FDA)

The FDDS Controller Adapter (FDA) provides the necessary electronics to accomplish track selection, head loading, format recognition, data transfer, error detection, host interface operation, status reporting and format generation. All functions of the FDA are performed under the control of the FDA's microprocessor.

Operations are broken into simple macros which allow flexibility of using software and systems hardware with the FDA carrying out the detailed micro steps internally.

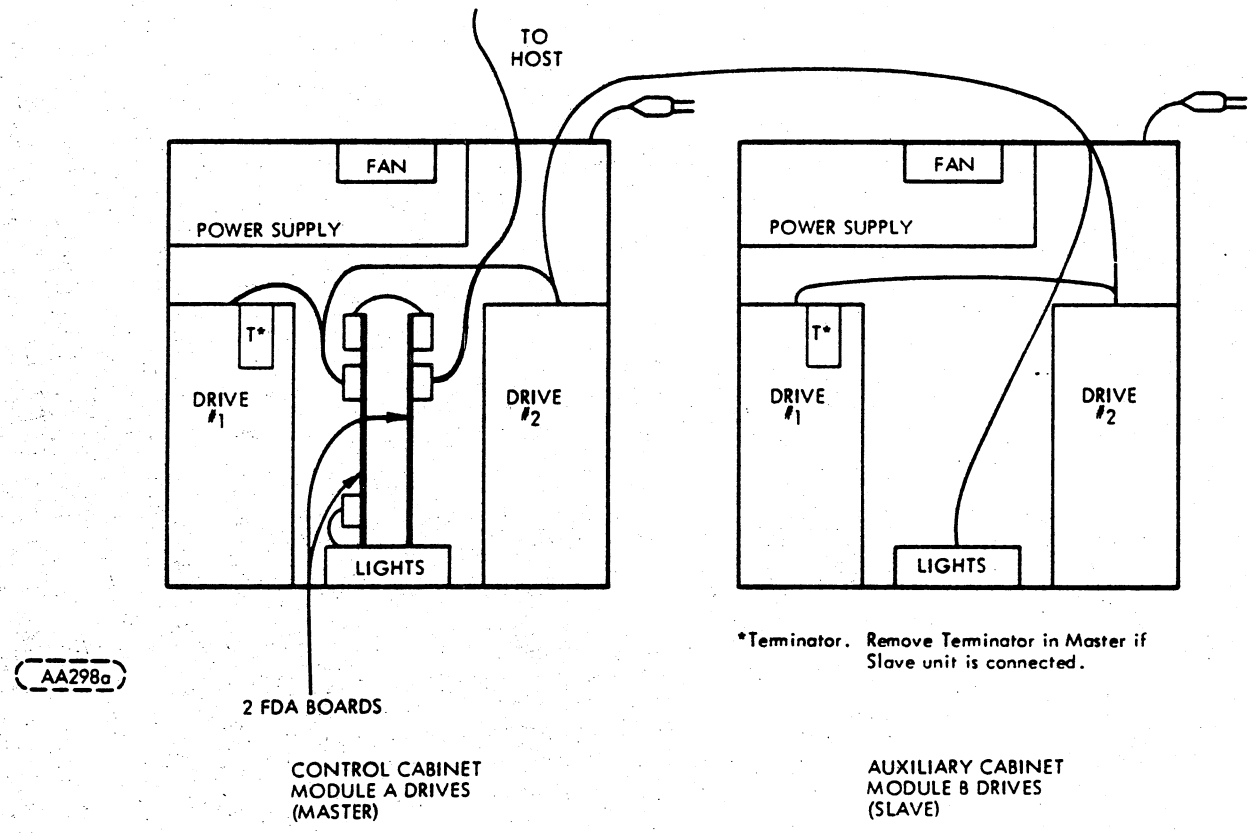


Figure 1-1. FDDS Framework

The functions internal to and performed by the FDA are as follows:

1. Head Positioning Function

   A. Stores actual address.

   B. Stores desired address.

   C. Compares desired and actual address and generates the proper pulses and direction to obtain the desired track.

   D. Recognizes bad tracks as initialized and provides compensational positioning to the proper track.

2. Timing Functions

   A. Write oscillator.

   B. Phase Lock Oscillator for MFM and Double Frequency.

   C. Index pulse monitor (for FDD door opened and command control).

   D. Fixed timeouts for head load and move. The head load is independent of the Host. The Host issues a command such as Read, Write or Restore and the FDA will automatically load the head, complete the I/O function and unload the head at the end of four index revolutions if no I/O command follows the initial function command.

   E. Read/Write splice timing.

3. Data Recovery

   A. Frames cell time (determine clock and data).

   B. Frames clock and data in bytes for D.F.

   C. Frames data in bytes for MFM.

4. Format Handling

   A. Writes sync separator characters and their clock patterns.

   B. Recognizes 3740 addressing format.

   C. Checks or generates CRC for data field.

   D. Writes, recognizes and indicates deleted records.

   E. Writes format on disk.

   F. Provides variable sector size format.

5. Header Data Handling

   A. Recognizes, verifies and responds to IBM 3740 format (single density) or CDC double density format.

   B. Declares an error if CRC is wrong.

   C. Indication given when address cannot be found.

   D. Initiates write or read when correct address is found with verification of the address and CRC.

   E. Accommodates variable length sector size defined by header data.

6. Read Data Message Handling

   A. Recognizes data field sync character.

   B. Provides a 256 byte buffer.

   C. Informs the Host when disk operation is complete.

   D. Declares an error when Host fails to maintain the transfer rate for lengths greater than 256.

   E. Evaluates the CRC and declares an error if not a valid compare.

7. Write Data Message Handling

   A. Provides a 256 byte buffer. (Full 128 bytes for sector size 128 or full 256 bytes for sector size greater than or equal to 256 must be transferred for a write operation.)

   B. Writes Data field sync character and its clock pattern.

   C. Declares error when Host fails to maintain transfer rate for sector lengths greater than 256.

   D. Write one bits after CRC.

8. Function Interpretation

9. Interface

   A. The FDDS Controller Adapter provides TTL interface to the Host and FDD (see Figure 1-2). Cable length should be 10 feet (3.05 m) or less to the Host and/or FDD.

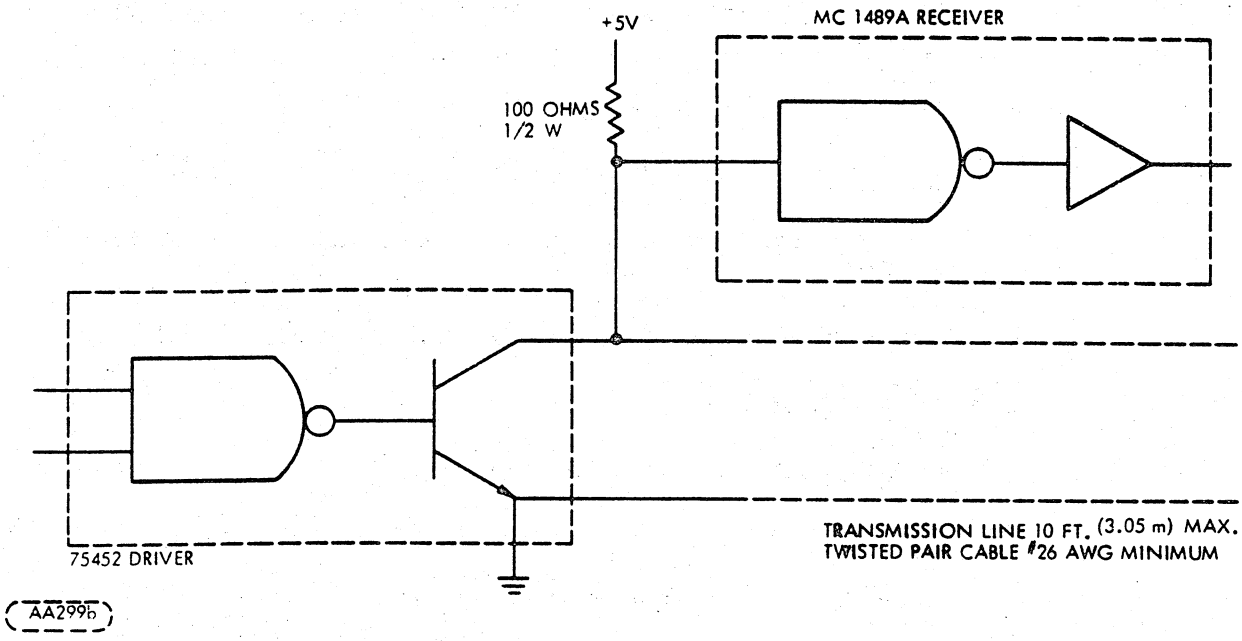


Figure 1-2A. Driver/Receiver Used for 8 Data Bus Transmission Lines To/From Host

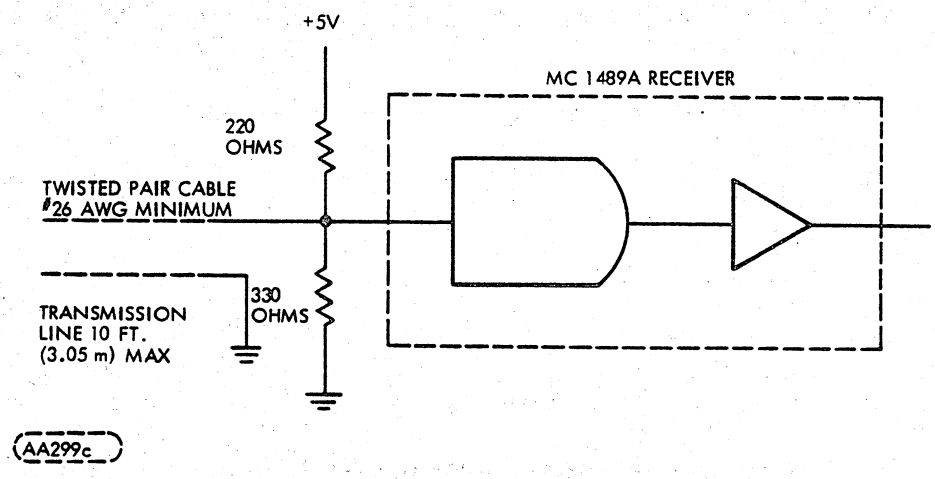


Figure 1-2B. Receiver Circuit Used for Inputs from Host

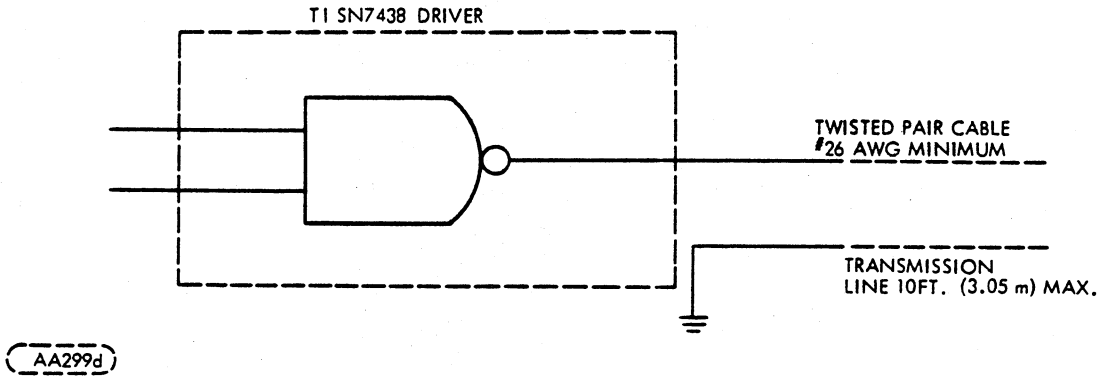


Figure 1-2C. Driver Circuit for Outputs to Host

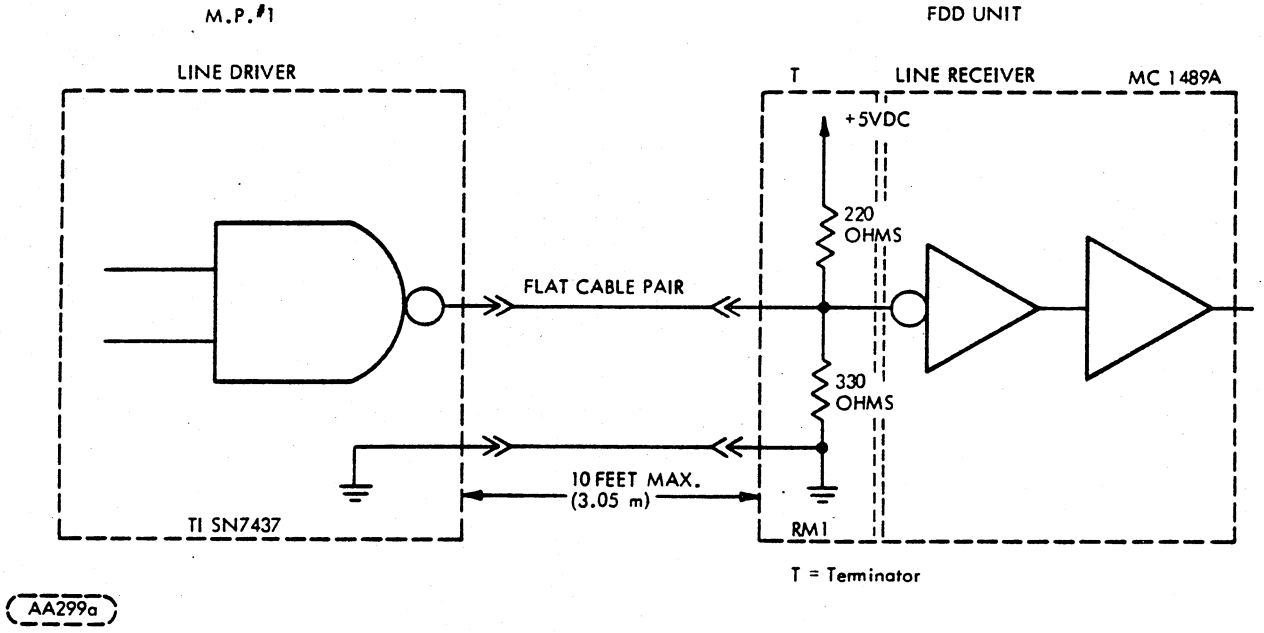


Figure 1-2D. Control/Data Transmission System To/From Microprocessor No. 1 and FDD Units

Logic Level = 0 = True (active low 0 to 0.5V) at the output/input of Line Driver, Line Receiver.

=1= False (+4.5 to +5.5V) at the output/input of Line Driver and Line Receiver.

T = Terminator on last drive only (#1 in Slave, or #1 in Master if Slave unit not in system).

1.4.4 POWER SUPPLY

The power supply provides all internal requirements for the FDA and two FDD units. The power supply is programmable for any AC source from 100 to 250V nominal at either 50 or 60 Hertz by means of tap selection on the transformer. The power supply is modular and field replaceable. For 50/60 Hertz conversion of the FDD, no changes are required for voltage changes and only a reversible pulley change is necessary.

The power supply will provide the following voltages:

+24V ±10% @ 5A
+5V ±5% @ 9A (2A available for customer interface)
-5V ±5% @ 0.6A
+12V ±5% @ 0.6A
-12V ±5% @ 1.0A

1.5 SYSTEMS CONFIGURATION

The FDDS requires only single phase AC power. A spare P.C. card space is provided in the Master unit to allow for customized FDDS/Host/I/O systems interfaces. The available spare will accommodate one 9" X 12" P.C. card (see Figure 1-3).

1.6 AC POWER

The FDDS requires single phase AC power 50 or 60 Hertz in a range of from 100 to 250V. The AC power connections and tap selections are shown in Figure 3-3.

1.7 PERFORMANCE CHARACTERISTICS

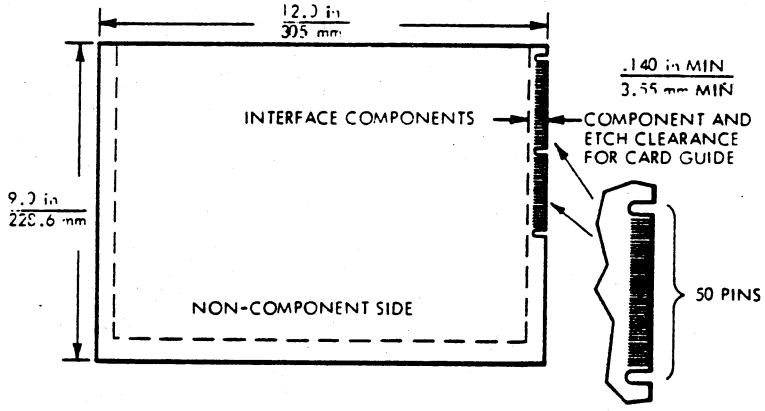
1.7.1 DATA CAPACITY

The FDDS utilizes two FDD units. Each 9404 (single-sided) FDD unit is capable of accepting the IBM 3740 diskette, the 421-60 (Single Density) or the 423-60 (Double Density) diskette. The 9406 (double-sided) FDD is capable of accepting the aforementioned diskettes plus the IBM double-sided diskette or the Control Data 425 double-sided diskette. When used with the 9474 FDDS, each drive can operate with variable length sectoring or CDC double density format. This format results in the following formatted capacities and configurations. (Not including one (1) spare track and two (2) alternate tracks).

	Single-Sided (9404)	Two-Sided (9406)
Usable diskette surfaces	1	2
Index tracks per diskette	1	2
Data tracks per diskette	73	146

SECTORS PER TRACK	26		15		8		4		2		1	
	SD	DD	SD	DD	SD	DD	SD	DD	SD	DD	SD	DD
Bytes per Sector	128	256	256	512	512	1024	1024	2048	2048	4096	4096	N/A*
Data Records per Diskette												
9404	1898	1898	1095	1095	584	584	292	292	146	146	73	N/A*
9406	3796	3796	2190	2190	1168	1168	584	584	292	292	146	N/A*
Data Bytes per Diskette												
9404	242K	485K	280K	560K	299K	598K	299K	598K	299K	598K	299K	N/A*
9406	485K	970K	560K	1120K	598K	1196K	598K	1196K	598K	1196K	598K	N/A*

*An 8192-byte sector exceeds the error detection effectivity of the 16-bit (X^{15} polynomial) CRC generation/checking logic.



AA281-2

1. Maximum component height from card -0.75 in. (19.1 mm).
2. Interface connector mounted on Right Side of card as shown.

Figure 1-3. Customer Card

1.7.2 DATA TRANSFER

1. Read/write data transfer is accomplished through a 256 byte data buffer.

2. When writing to disk 128 bytes must have been transferred to the FDA for sector length of 128 and 256 bytes must have been transferred to the FDA for sector lengths of 256 bytes or greater. If writing sector lengths greater than 256 bytes, the remaining bytes must be transferred at least as fast as the bytes are recorded (i.e., at an average rate of 32 us/byte for single density of 16 us/byte for double bit density).

3. When reading from the FDA, it is not required to read the entire record, however, the buffer must be cleared for the next disk function. The read/write buffer is cleared only on power up, master clear, write buffer function and by the host failure to maintain the transfer rate (i.e., 32 us/byte for single density of 16 us/byte for double bit density) when sector length is greater than 256 bytes. When reading only a partial buffer it is recommended that the host issues a write buffer function without data transfer to clear the buffer.

1.7.3 ERROR DETECTION

1. Error checking by CRC on the address field and CRC on the data field.

2. Error indications are transmitted to the Host as a status byte when requested. The FDA will flag an interrupt, the Host may request status or ignore it. Interrupt will remain active unless a Status Request or Master Clear is issued.

3. Programming Considerations - Read after write will be firmware or software performed by the user and not automatically generated in the FDA.

4. To guard against degradation from imperfections in the media, it is recommended than no more than 4 attempts to write a record be used when read after write errors are encountered. In the event a record cannot be successfully written within 4 attempts, it is recommended that the sector or track be labeled defective and an alternate sector or track assigned. If more than 2 defective tracks are encountered, it is recommended that the disk be replaced.

5. In the event of a read error up to 10 attempts should be made to recover with re-reads. If after 10 attempts the data has not been recovered, initiate a restore or issue a read of another track several tracks away and reposition to recover the data. If the error persists, the restore/reposition sequence should be attempted at least 10 times.

1.8 TRANSPORTABILITY

The Flexible Disk Drive Subsystem because of its relatively small size and light weight may be moved by hand within the general area of operation. When moved any distance the unit should be packed for shipment.

1.9 DURABILITY

The Flexible Disk Drive Subsystem is packaged to withstand normal handling.

1.10 EMI/RFI PROTECTION

The FDDS will provide EMI/RFI protection on the incoming AC power line.

1.11 MAINTAINABILITY

1.11.1 ACCESSIBILITY

The flexible disk drive modules are directly accessible.

1.11.2 ADJUSTMENT

Instructions are provided in Section 6 for adjusting the clock VFO should it be required. The need for adjustment should be rare, however.

1.11.3 MAINTENANCE PHILOSOPHY

On-site module replacement.

Repair Center replacement on the component level.

1.11.4 INTERCHANGEABILITY

No restrictions on media interchange from unit to unit.

1.11.5 SPECIAL EQUIPMENT

On Site

FDDS - No special tools required.
FDD - See FDD Product Specification.
Repair Center - CE alignment tool for alignment of index transducer and track 00 DC CDC part number 74290000 and carriage stop adjustment tools, part numbers 83401300 and 83401400.
Oscilloscope.

1.12 SAFETY

The Flexible Disk Drive Subsystem uses no DC power in excess of 40 Volts. The primary power circuit is fuse protected. A third conductor in the AC power cable provides a chassis safety ground.

1.13 HUMAN ENGINEERING

Human interface is minimal. A power on switch/indicator is provided. Unit active lights are used to display the unit currently active to the host computer to discourage accidental operator interference. To load the media the operator opens the access cover and inserts the disk into a slot in the front of the unit. The access cover is then closed. Disk change is allowable in the unused unit while the other is active.

CAUTION

Load and unload media ONLY when power is on the unit.

II
OPERATION

2.1 SCOPE

This section provides the instructions and information required to operate the FDDS unit.

2.2 CONTROLS AND INDICATORS

Figure 2-1 depicts the locations of the controls and indicators. A functional description of the controls and indicators is given in Table 2-1. Operation of the FDD is given in the FDD manual which is included with each FDDS unit. The controls and indicators are identical for both Master and Slave units.

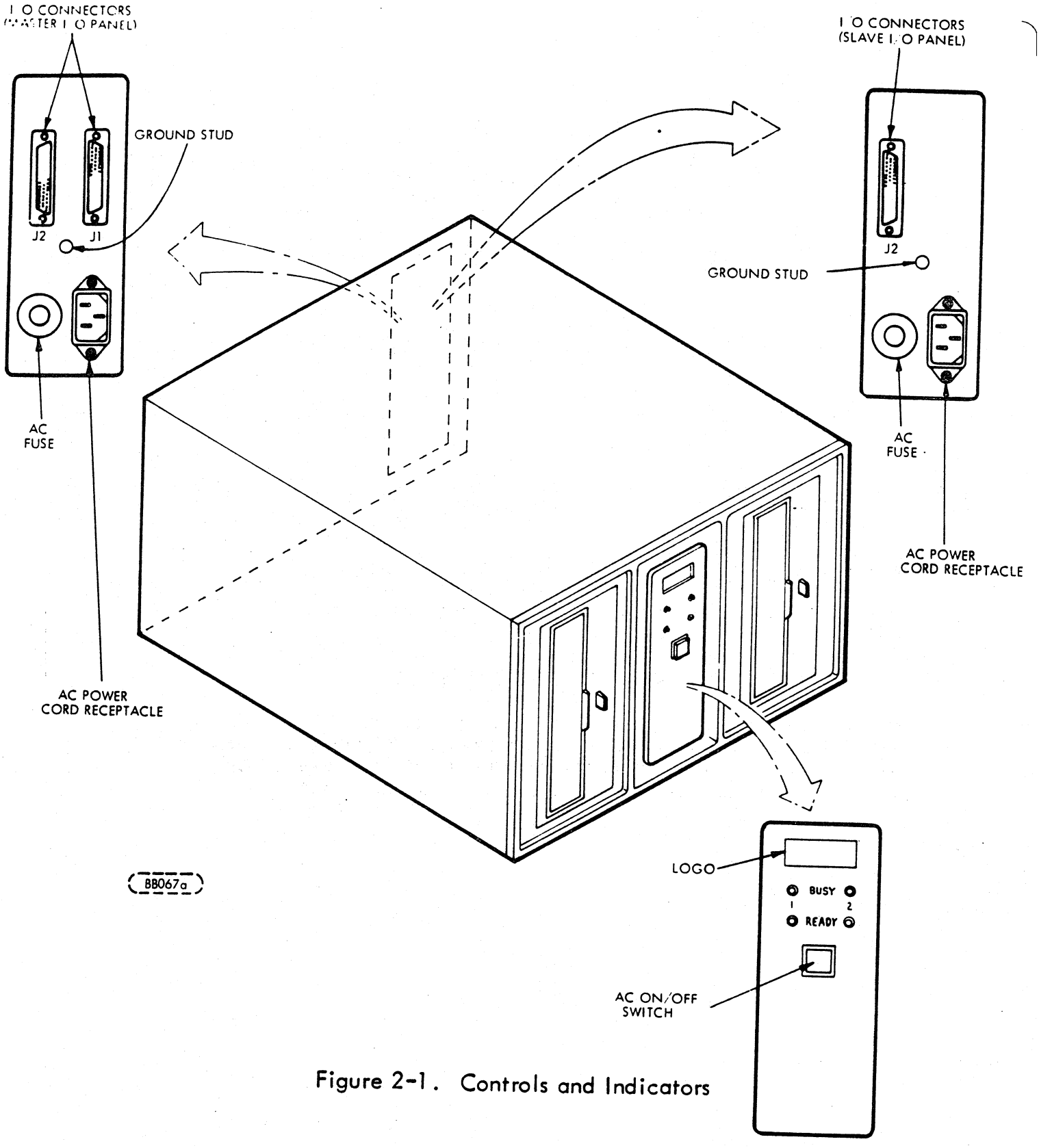


Figure 2-1. Controls and Indicators

Table 2-1. Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
POWER ASSEMBLY	
AC fuse	Provides AC power circuit protection.
Power receptacle	Provides connection for AC input power.
Voltage adjust plug (refer to Installation and Checkout Section for adjustment instructions)	Provides a means of selecting input voltage to transformer in power supply.
CONTROL PANEL	
ON/OFF indicator/switch	The ON/OFF switch operates a relay which connects the AC power to the FDDS power supply and the two FDD units. The switch is in the "in" position and the indicator illuminated as long as AC power is on. Depressing the switch releases the relay thus removing AC power from the unit.
BUSY indicator (1 & 2)	When illuminated shows that disk functions are being executed (not including READ BUFFER, WRITE BUFFER or STATUS REQUEST) on the indicated unit.
READY indicator (1 & 2)	When illuminated shows that the selected drive has media in place, door closed, and media up to speed.

III
INSTALLATION AND CHECKOUT

3.1 INTRODUCTION

This section provides the information and procedures necessary to install the Flexible Disk Drive Subsystem.

3.2 UNPACKING

During unpacking, exercise care so that any tools being used do not cause damage to the unit. As the unit is unpacked, inspect it for possible shipping damage. All claims for this type of damage should be filed promptly with the transporter involved. If a claim is filed for damages, save the original packing materials.

After unpacking the unit remove the cover on desk mount units by removing the two screws at the lower rear of the cover and carefully sliding the cover rearward. On rack mount units remove one screw on each side and lift cover off.

Visually inspect the unit and insure that the PWB's are properly located in the bottom notches and upper board guides. Insure that all internal cable connectors are properly mated with their respective connector (see Figure 3-4).

3.3 SPACE ALLOCATION

Figure 3-1 shows the unit overall dimensions for determining space allocation. In addition, Figure 3-2 gives detail dimensions for rack mounted units.

3.4 INSTALLATION AND MAINTENANCE

Required connections to the device are power/signal cables and system ground consistent with normal peripheral equipment grounding practices. The physical requirements are adequate clearances for maintenance and air intake/exhaust. Detailed instructions for maintenance are found in Section 6 of this manual and FDD Manual.

3.5 POWER REQUIREMENTS

3.5.1 AC VOLTAGE

The FDDS (both Master and Slave) requires single phase AC power 50 or 60 Hertz in a range of from 100 to 250V. The AC power connections and tap selections are made by changing jumper positions of Jumper Plug J25 located inside the power supply assembly. See Figure 3-3 for diagram and table showing these adjustments. Before operating the FDDS insure that the input power circuitry of the unit is configured to receive the power to be applied to the unit. Figure 7-1 shows the location of J25.

At 120V 60 Hertz the unit draws 3.5 amps.

CAUTION

If converted from 120V 60Hz to any other voltage and/or frequency REMARK LABEL.

3.5.2 OPERATING FREQUENCY CONVERSION

If the required operating frequency is different than that which the unit is different than that which the unit is configured, the procedure for converting operating frequencies is given in Section 6.8 of the FDD Manual.

3.6 POWER CABLE

The AC power cable plugs into the lower right corner of the I/O and AC bracket at the rear right of the FDDS unit. The characteristics of the AC power cable should be as described in procurement specification 75778700, which described the characteristics of cables for use with several different voltages and both 50 and 60 Hertz.

CAUTION

When units are field configured for any line voltage other than 120V, the CSA Certifications Marker must be removed from the equipment in order to comply with requirements of the Canadian Standards Association.

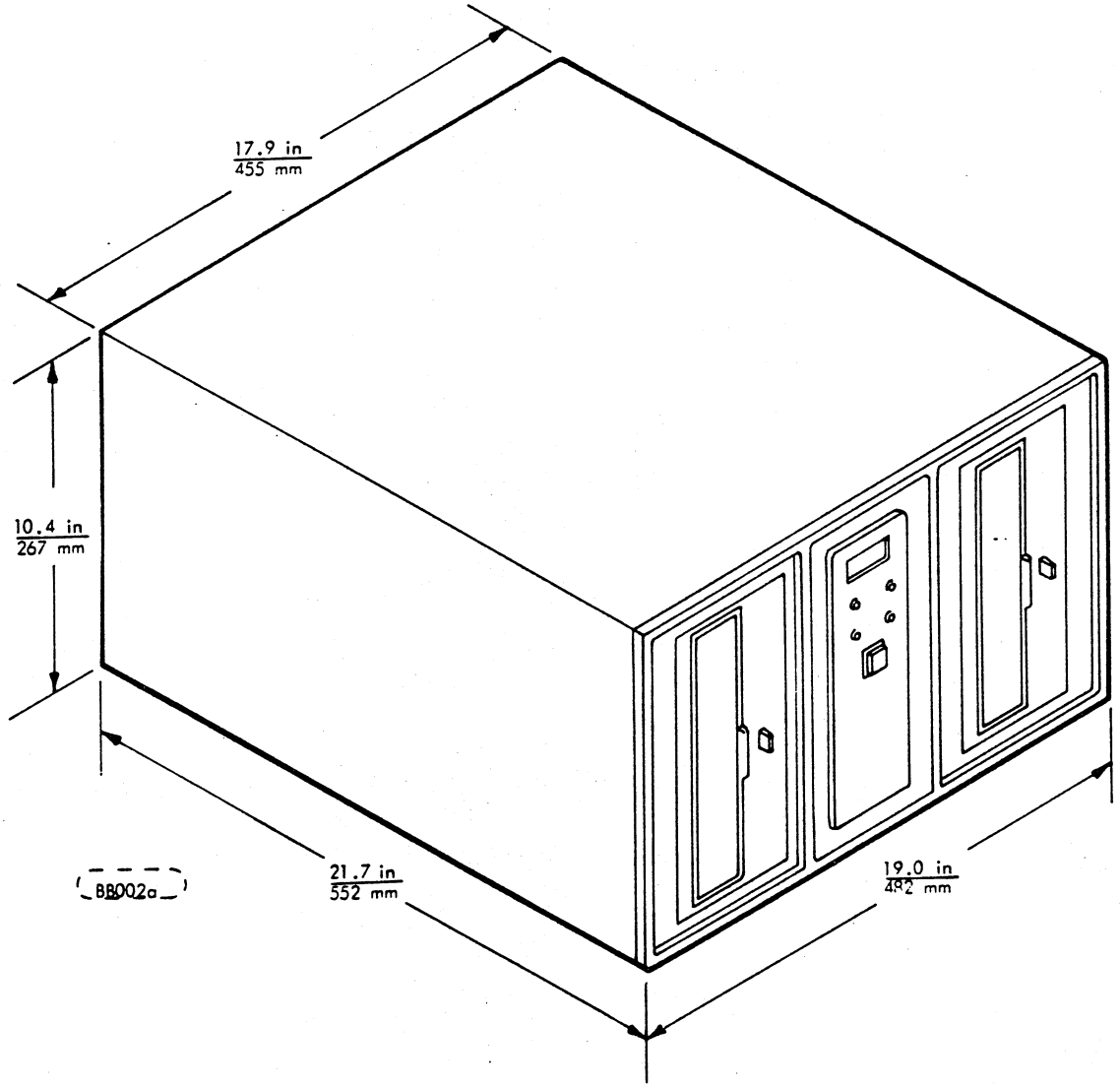
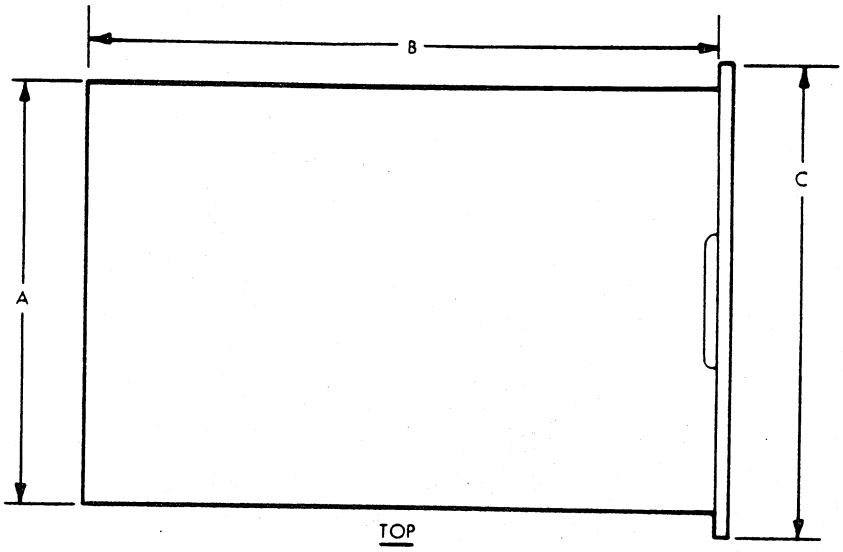
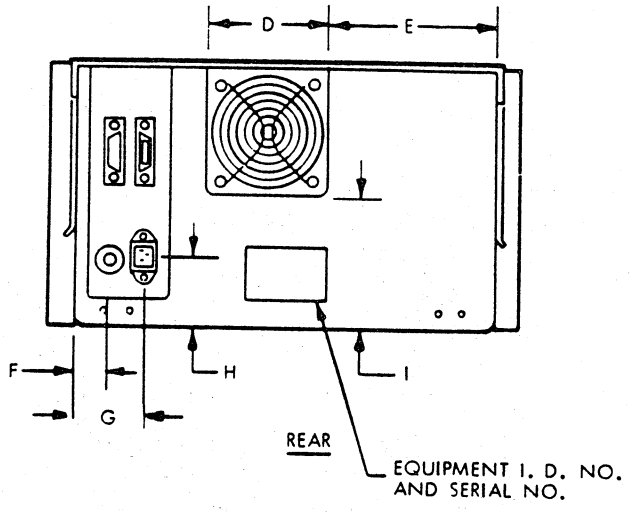


Figure 3-1. Base Cabinet Dimensions





INDEX LETTER	DIMENSIONS	
	in	mm
A	17.1	434
B	21.3	541
C	19.0	482
D	4.75	121
E	6.95	177
F	1.15	29
G	2.65	67
H	2.5	65
I	4.65	118
J	1.5	38
K	5.25	133
L	5.5	144
M	4.25	108
N	5.0	127
O	1.25	32
P	10.4	264

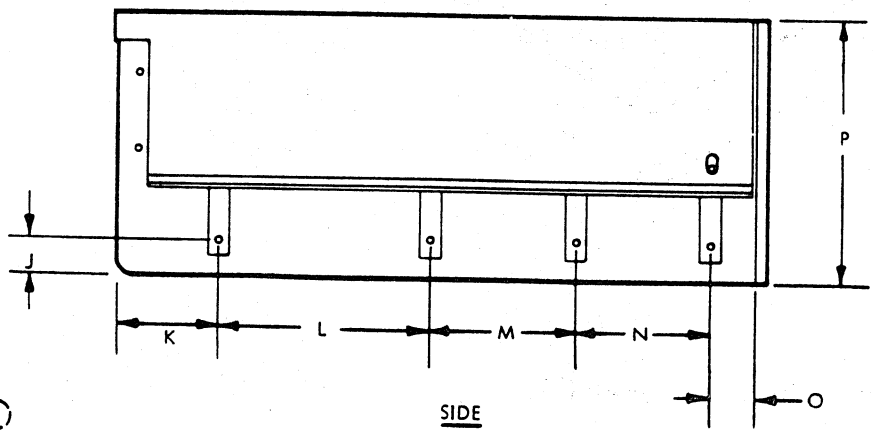


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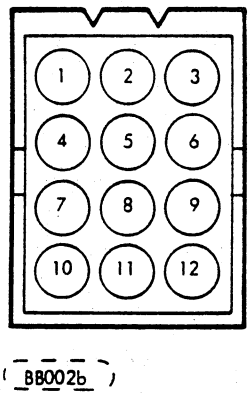
Figure 3-2. Detailed Dimensions



J25
(View from Jumper Side)

NOMINAL VOLTAGE	VOLTAGE RANGE	JUMPER PLUG J-25	JUMPER PLUG P/N
100	90 - 107	(1&7) (2&8&12)	77830721
120	104 - 127	(1&7) (3&9&12)	77830722
200	180 - 213	(2&7) (8&4&12)	77830723
220	198 - 235	(3&7) (8&12&4)	77830724
230	207 - 246	(2&7) (4&9&12)	77830725
240	216 - 257	(3&7) (9&4&12)	77830726
250	225 - 268	(3&7) (10&4&12)	77830727

See Figure 7-1 for location of J25.

Figure 3-3. Input AC Power Connections Tap Selections

3.7 CABLING AND CONNECTIONS

All input/output (including power cables exit at the rear of the FDDS unit. Refer to Figure 5-1 and 5-2 for connector pin/signal assignments for these cables. It should be noted that if a user circuit card is installed in the Master FDDS unit, the signal names given for J1 and J3 of the I/O board in Figure 5-1 do not apply. Names given to those signals by the user would apply. The function of each signal name shown in I/O J1 in Figure 5-1 is described briefly in Table 3-1 and in more detail in paragraph 4.2. The cable length for the cable which would plug into I/O J1 should not exceed 10 feet (3m) Figure 5-1 applies to the Master FDDS unit and 5-2 applies to the Slave. The cable which connects the Master to the Slave is documented in the Parts Data Section, Section 8, and is provided with the Slave unit. If the Host circuit board is installed in the Master cabinet, the user provides the cable required to interface to J3 of the I/O board.

3.7.1 SIGNAL LINE TERMINATOR

When the FDDS units are shipped there is a terminator resistor module RM1 installed on the Component Board Assembly of FDD Drive #1 of both the Master and the Slave units. If the FDD units in the Slave unit are connected to operate daisy chain with the FDD units in the Master, the terminator module (RM1) should be removed from FDD Drive #1 of the Master unit. The FDD maintenance manual shows the location of RM1 in the FDD component Board Assembly parts layout figure in Section 5 of that manual. If there is no Slave unit connected to the Master then the terminator module RM1 stays in Drive #1 of the Master. Whenever the system consists of a Master and Slave unit the Slave power must be on when the Master power is on, whether or not the Slave is to be used. This provides power for the terminators.

3.7.2 FDDS/HOST EXTERNAL INTERFACE

The connector required to interface the external Host I/O cable to J1 of the FDDS is Amp P/N 205211-1 (or equivalent) using P/N 205090-2 (or equivalent) pins. This connector/cable must be supplied by the equipment user.

3.8 GROUNDING

3.8.1 SYSTEM GROUND CONNECTIONS

Frame ground and logic ground are isolated within the FDDS. It is not recommended that the user tie these two together within the FDDS. It is preferred that frame ground and logic ground be tied together at a single point in the user system. A check should be made before operating the FDDS in the user system to see that proper grounding has been accomplished.

NOTE

The I/O Option in certain FDDS configurations (see Table 8-1 and Figure 8-12) grounds to the frame on the I/O PWA each ground wire in the interface cable. This is true of the signal cable between the Host and FDDS and the cable between FDDS Master and Slave units.

3.8.2 FRAME GROUND

All parts of the FDDS frame and associated metalic parts are connected together through low impedance contacts. The power cord ground and the frame ground are tied together at a common point near the power supply on the inside base of the FDDS base frame. This common point is also tied to a ground stud on the I/O panel. If an additional system frame ground wire is needed, it should be connected to the stud on the I/O panel. The frame of Master and Slave units are tied together by the shield of interconnect cable which connects to a stud on the I/O panel.

3.8.3 LOGIC GROUND

The Flexible Disk Drive electronics and the FDD microprocessor electronics have a common logic (or DC) ground point. The logic ground and frame ground are isolated from one another. The isolation between logic and frame ground is greater than 1,000 ohms.

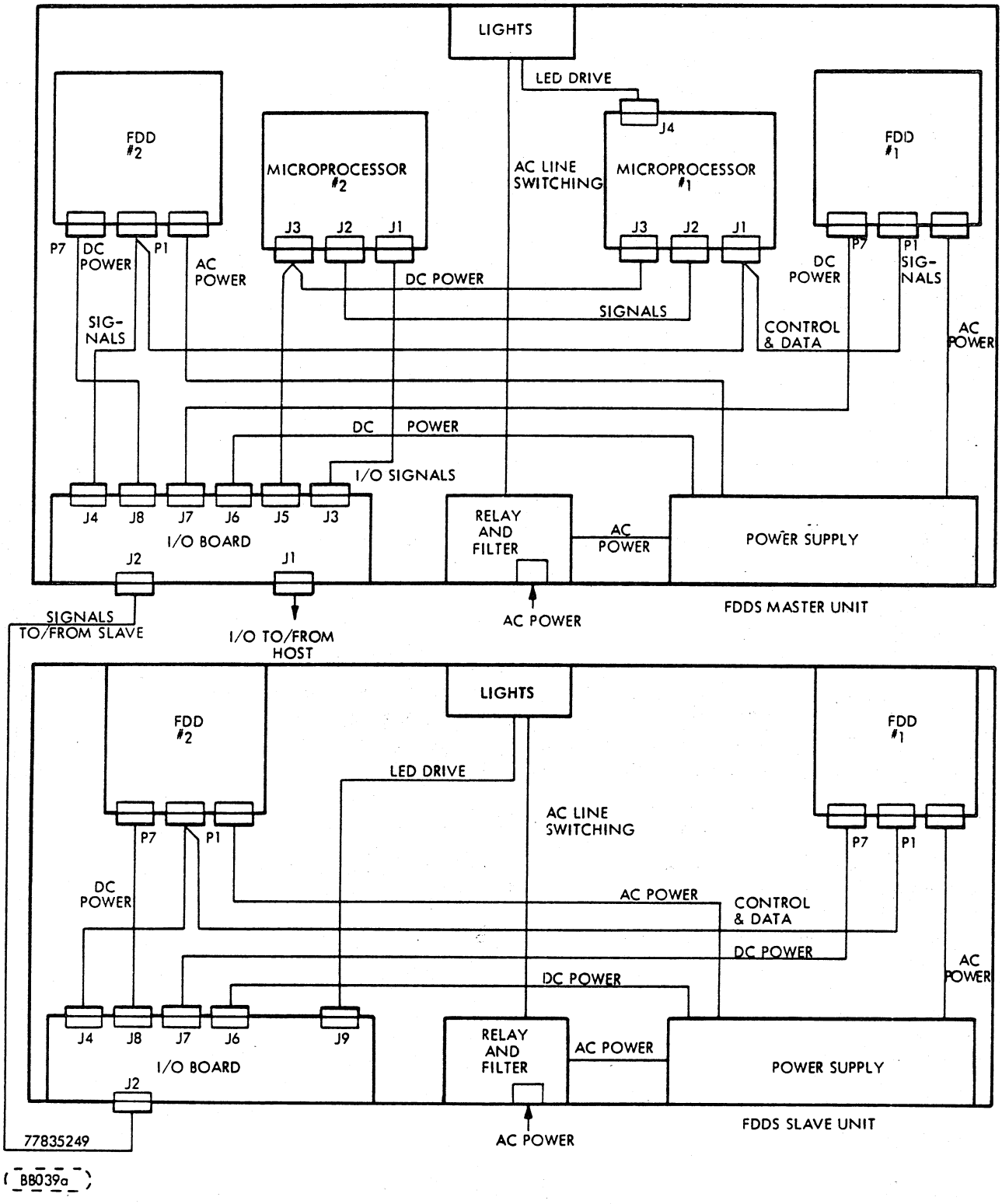


Figure 3-4. Simplified Internal Cabling Diagram

3.9 ENVIRONMENTAL LIMITS

3.9.1 TEMPERATURE AND HUMIDITY

The Flexible Disk Drive Subsystem can withstand the following conditions, if providing the combined rate of temperature and humidity change precludes condensation of moisture on any part of the unit.

	Operating	Storage and Transit
Temperature, °F	50° to 95°	-30° to 150°
Temperature, °C	10° to 35°	-35° to 65°
Temp. Change °/hr.	6.7°C (12°F)	33°C (60°F)
Relative Humidity	20% to 80%	5% to 95%
Max. Wet Bulb Temp. °F	79	
Max. Wet Bulb Temp. °C	26.1	

Refer to Specification for 421-60 and 423-60 Flexible Disk for media environmental limits.

Altitude (Actual or Effective)

- Operating - 1000 feet below sea level to 10 000 feet above sea level.
- Transit (as packed for shipment) - 1000 feet below sea level to 15 000 feet above sea level.

3.9.2 CLEANINESS

The Flexible Disk Drive Subsystem is designed for use in commercial and industrial environments. However, optimum performance can be expected when used in a computer room environment with the resultant air cleaniness normally found in such a location. Dust and other airborne contaminants are a major threat to the operating life of the media, head and positioning system.

3.9.3 DISK STORAGE AND HANDLING

The disk performs well when given reasonable care. The same handling specified for computer magnetic tape should be followed. Some specific areas are as follows:

When not in the unit, keep the disk in the protective envelope. Place the disk in the envelope before writing on the label so that the label is visible through the cut-away front of the envelope.

When writing on disk label care should be taken to use a felt tip pen. Ball point or pencil will impregnate the oxide on the media and pencil lead fragments will contaminate the media.

Always handle the disk by the label area to avoid touching the mylar surface.

Keep all magnets away from disk. Magnetic fields can destory recorded data on the disk.

Do not touch or attempt to clean the disk surface. Abrasion may result in loss of stored data.

CAUTION

Load and unload media ONLY when power is applied to the unit.

3.10 COOLING

Cooling air is drawn in at the front of the unit and exhausted through the rear by the fan. A minimum of 1 1/2 in. (38 mm) clearance must be provided at the rear of the unit to maintain unrestricted air flow. A positive pressure near the rear exhaust should not exceed 0.03 inches of water (7.47 Pascal).

3.11 COMMUNICATIONS WITH HOST/INTERFACE

That part of the FDDS which communicates with the Host is called the Adapter or FDA. The Host may be within or external to the FDDS. *

Communication between the FDA and the Host is accomplished by 16 interface lines: 4 lines for control signals from Host to Adapter, 4 lines for status signals from Adapter to Host, and 8 data lines for bidirectional use by both Host and Adapter. Signal names, direction of data flow, and type of information transmitted are presented in Table 3-1. Signal requirements are defined in detail in Paragraphs 4.2.1 through 4.2.8.

Table 3-1 lists the I/O Line signal names and gives a brief description of what each does. A detailed description is given in Section 4.

*The users may install a Host circuit board in the extra board slot of the Master FDDS.

3.11.1 FUNCTION CONTROL

When the Host issues a legal function code (11 on the tag lines), the FDA will execute the control function coded on the data lines, unless a function is already in operation. The control functions are listed in Table 3-2 and discussed in more detail in Section 4.

NOTE

The FDA strobes a function into its internal latch during Data Enable and before Data Strobe.

3.11.2 STATUS REQUEST (DM01 0000)

When the FDA is Busy the Host may issue a Status Request at any time to the currently selected drive without affecting any existing operation. When the FDA is not Busy, the Host may issue a Status Request to any drive. A Status Request will normally be issued upon receiving an Interrupt from the FDA. If a Status Request is issued to a non-selected Drive while FDA is Busy, there will be no response to Data Enable.

3.11.3 STATUS INTERPRETATION

When the Host issues a Status Request, the FDA will respond with status information coded on the data lines. Status conditions are described in Section 4. Status codes are listed in Table 3-3.

Table 3-1. Input/Output Lines*

SIGNAL NAMES**	FUNCTION
	Input Lines
TAG 1 TAG 2	The Tag codes define the type of information on the data lines.
DATA ENABLE	Indicates data and tag lines are stable and information is available to the FDDS, or indicates a request for the FDDS to put data byte or status code on the data lines.
HOST DATA 0 through HOST DATA 7	Bi-directional data lines used by both FDDS and the Host. TAG lines define the type of information on these lines.
MASTER CLEAR	Signal to the FDDS to reset the buffer pointer (in the Master), and (if present) return Slave Drive #2 to track 00, followed by Slave Drive #1, then Master Drive #2, followed by Master Drive #1, leaving Master Drive #1 selected.
	Output Lines
DATA STROBE	Signal from FDDS to Host which acknowledges Data Enable from the Host and indicates that the FDDS has accepted the information on the data lines or has placed data on the lines.
INTERRUPT	Used to request data transfer, indicate an operation is complete, or together with BUSY call attention to an error condition.
BUSY	The Busy line is set while executing all control functions to a disk drive (except Read Buffer, Write Buffer, Status Request, Mode Set and Module Select), and remains set if an error condition occurs.
READY	Active during the time a disk drive is selected if the selected drive is detecting index pulses at the proper speed.

*See paragraph 4.2 for the details on these I/O signals.

**Names applicable at J1 of Microprocessor #2. Signal names at J1 and J3 of the I/O Board are determined by the user system if a Host board is mounted in the FDDS.

Table 3-2. Input Control to FDA (Functions)

FUNCTION	TRANSMITTED BY	TAG
1. Data	Tag lines 2 and 1	00
2. Function	Tag lines 2 and 1	11
3. Track	Tag lines 2 and 1	01
4. Sector	Tag lines 2 and 1	10
5. Data Enable	Line 3	
6. Master Clear	Line 5	

FUNCTION	TRANSMITTED BY	CODE* 18 11 MSB/LSB	REF. SECTION
7. Restore	Lines 11 - 18	D000 0000	4.2.9.6
8. Write Disk	Lines 11 - 18	DS00 0001	4.2.9.7
9. Read Disk	Lines 11 - 18	DS00 0010	4.2.9.8
10. Write Deleted Record	Lines 11 - 18	DS00 0100	4.2.9.10
11. Write Buffer	Lines 11 - 18	0000 1000	4.2.9.11
12. Status Request	Lines 11 - 18	DM01 0000	4.2.9.12
13. Read Buffer	Lines 11 - 18	0010 0000	4.2.9.9
14. Format Media	Lines 11 - 18	D001 0001	4.2.9.5
15. Module Select	Lines 11 - 18	M001 0100	4.2.9.1
16. Set Mode	Lines 11 - 18	0001 1000	4.2.9.4

*M Denotes module select address - Zero (0) for Module A, one (1) for Module B.

*D Denotes Device Address within a module - Zero (0) for Unit 1, One (1) for Unit 2.

*S Denotes whether RDT Bit is set.

Table 3-3. Status Codes Output from FDA

STATUS	TRANSMITTED BY	CODE* 18 11 MSB/LSB
1. Data Strobe	Line 4	
2. Interrupt	Line 8	
3. Ready	Line 9	
4. Busy	Line 10	
5. Operation Complete	Lines 11 - 18	0000 0001
6. Illegal Code Rec.	Lines 11 - 18	1000 0010
7. Deleted Record	Lines 11 - 18	0000 0100
8. Write Fault/Write Protect	Lines 11 - 18	1000 1000
9. CRC Error	Lines 11 - 18	1001 0000
10. Access Error	Lines 11 - 18	1010 0000
11. Request Data Transfer	Lines 11 - 18	1100 0000
12. Busy	Lines 11 - 18	1000 0000
13. Idle	Lines 11 - 18	0000 0000
14. Not Ready	Lines 11 - 18	1111 1111
15. Buffer Overload/Underload	Lines 11 - 18	1000 0011
16. Transfer Timing Error	Lines 11 - 18	1000 0110
17. Format Track Over/Under Flow	Lines 11 - 18	1000 1110

*Status codes may overlap.

3.12 INITIAL CHECKOUT AND STARTUP PROCEDURE

This procedure should be used to determine that the FDDS is operational. The procedure can be performed whether or not the I/O cable to the Host is connected. Only the AC Power cable need be connected. The preceding procedures and requirements of this section should have been performed. If the system consists of a Master and Slave unit the cable connecting the two should be installed. Comments below apply to both Master and Slave.

1. Check that the power switch on the front panel is OFF.

2. Remove the top cover.

3. If it hasn't already been done check that the interior of the unit is clean.

4. Make certain that the input power cable is connected to the correct AC source.

5. Before turning on the power, carefully move the carriage assembly of each FDD to its forward most (or near so) position (away from the stepper motor) by turning the aft part of the actuator shaft (reference FDD manual Figure 6-18). Be careful not to damage the plastic stop on the shaft.

6. Depress the Power On switch on the front panel of the Slave first then the Master and watch the two actuators to be sure that Master Clear which occurs at power on brings the carriage back to what appears to be track 00, first on Drive #2 then on Drive #1 of the Slave (if present), then Drive #2 then Drive #1 of the Master. Whenever a Slave unit is connected in the system its power must be on when the Master power is on, whether or not the Slave is to be used. This is necessary to provide power to the terminators.

7. Check to see that the FDD spindles are rotating and that the blower is operating.

8. Insert a diskette in FDD #1 (left side and close the door). Figure 2-1 in the FDD manual shows how. The #1 READY indicator should turn on. Insert the diskette in FDD #2 (right side) and close the door. The #2 READY indicator should turn on.

CAUTION

A diskette should be inserted or removed ONLY when power is on.

9. Remove power from the units.

IV
THEORY OF OPERATION

4.1 INTRODUCTION

The theory of operation is described in terms of the major functions that the FDDS performs during normal and emergency operation and the circuitry and hardware involved in the performance of these functions. These functions are listed in section 1.4.3. Signal names are preceeded by the symbol "+" or "-" indicating that the active level of the signal is high (+) or low (-) respectively. For example, the signal -MEM WRITE indicates the signal is at a logic low level when active. Signals which leave the board/assy to which a particular schematic applies leave through a connector and the standard connector symbol applies, namely, the ——⟩⟩—— symbol. Figure 5-1, and 5-2 shows how all the boards/assemblies are connected together. Use it to follow signals from board/assy to board/assy. Further information how to read the schematics together with timing charts for the individual logic elements used is given in Section 5.

Refer to the applicable schematic, block diagrams, and timing charts for the following discussion.

Circuit board abbreviations used in this description are as follows:

M. P. 1 = Microprocessor Board number 1
M. P. 2 = Microprocessor Board number 2

See section 5.4.5 for a list of other abbbreviations used.

"HOST" could be external to the FDDS or it could be a circuit board installed in the FDDS by the user.

4.2 HOST/ADAPTER I/O SIGNALS

Table 3-1 in Section 3 gave a brief description of the I/O signals. This section will describe those signals in more detail. Interface connector pin/signal assignments are given in Figure 5-1 in section 5. These assignments are only valid if the Host is not physically located within the FDDS cabinet. The signal names apply at the input to Microprocessor #2 whether or not the Host is in the cabinet.

Paragraphs 4.2.1 through 4.2.8 describe the operation of the FDDS/Host interface. Figure 4-1 shows a typical timing sequence for a write cycle. Additional timing sequences are given in Appendix A.

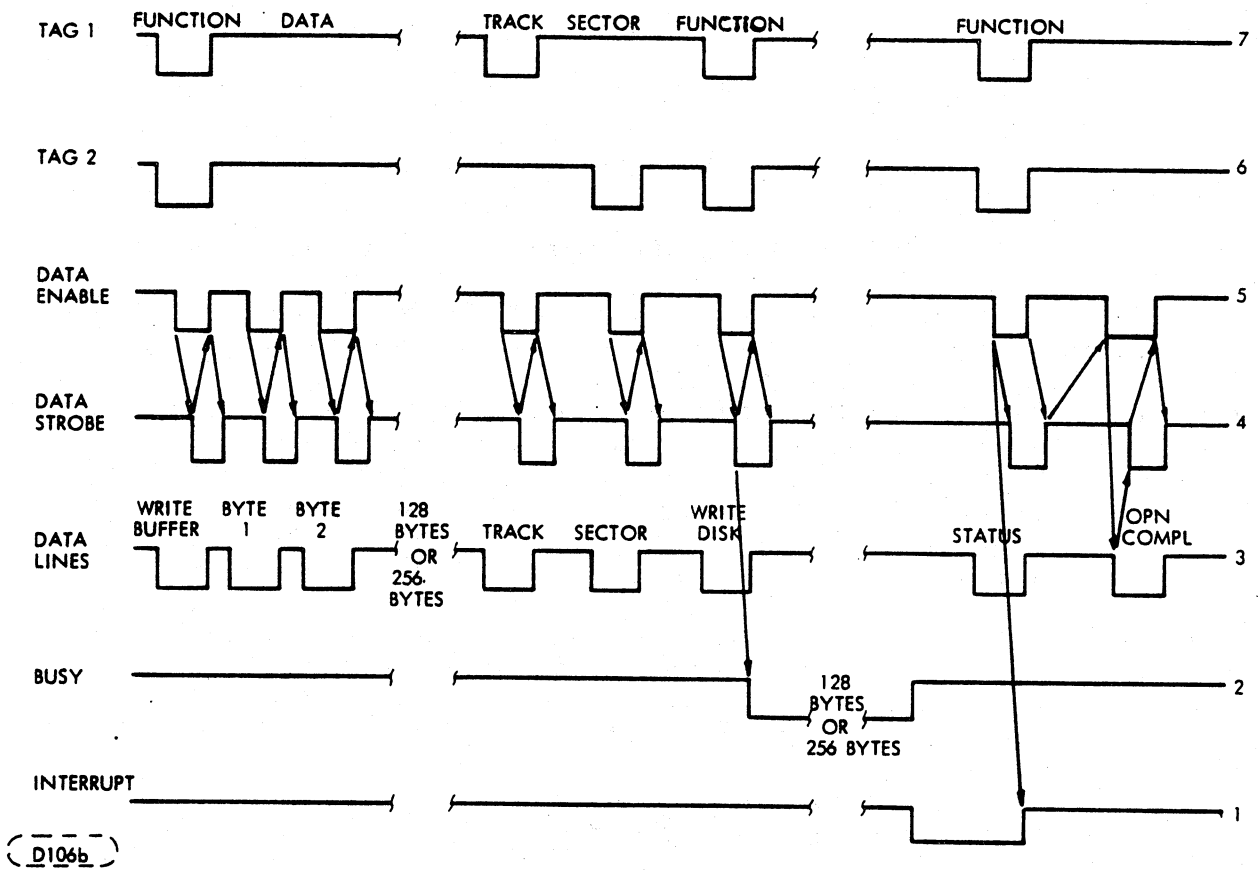


Figure 4-1. Single Write Cycle Timing

4.2.1 MASTER CLEAR

After receiving a Master Clear command, the Adapter will reset the Buffer pointer, return Drive #2 of Module B to track 00, followed by Drive #1 of Module B, then repeat process for Module A, leaving Drive #1 of Module A selected. The Adapter will issue a busy signal. At the completion of Operation the Ready Line is dependent on the condition of Drive #1 Module A and the Not Ready status is dependent on that drive. When the heads are restored to track 00, Busy will be terminated. If any head does not reach track 00 within a predetermined time, the Restore for the Drive is aborted, and the Master Clear operation is continued. The adapter will then assume Idle status with mode definition of Single Density and Buffer size equal to 128 bytes.

Initial Power-up will also initiate a Master Clear for all drives. An interrupt will not be flagged after completing a Master Clear (Master Clear activated by Master Clear line or during power-up).

The Host may issue a Master Clear at any time, even when the Adapter is busy. After a Master Clear, the track and sector values must be sent or the Adapter will respond with Illegal Code to a disk function.

Master Clear Timing Sequence is shown in Figure 4-2.

NOTE

It is imperative that NO data transfer type operation take place concurrently with a Master Clear Function.

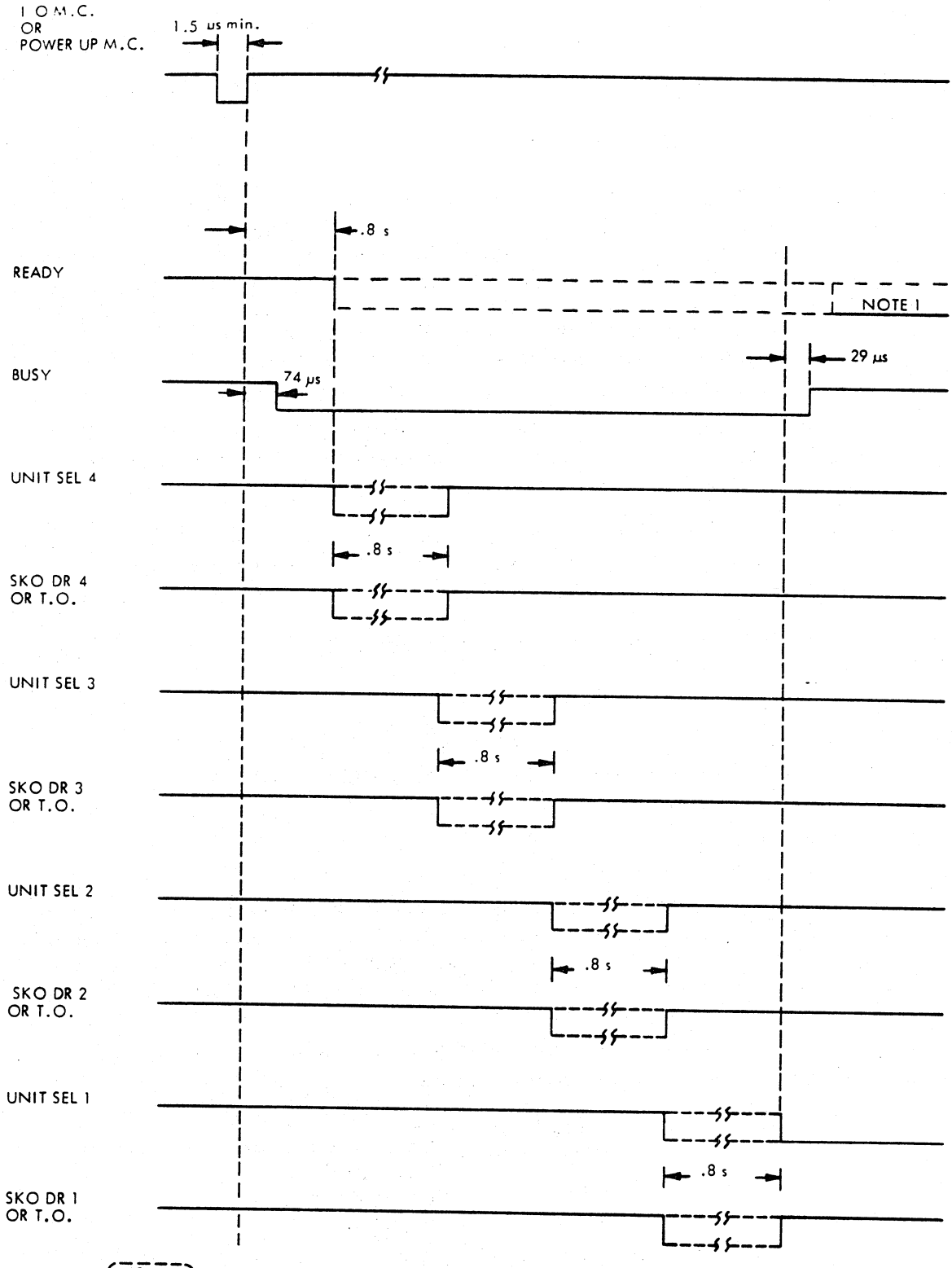
4.2.2 TAG LINES

The Tag codes define the type of information on the data lines and may be transmitted in any sequence, except that the Disk Access function must be the last in the sequence. The tag lines from the Host must be active and stable when Data Enable is activated and must remain active and stable until Data Enable is deactivated. This is true for all data, function or status transfers.

Four Tag codes, consisting of two bits each will be transmitted to the Adapter over the two tag lines. The Tag codes are as follows:

TAG 2	TAG 1	
0	0	Data, Status Code
0	1	Track Address
1	0	Sector Address
1	1	Function

Data, track, sector, and function information can be transmitted only when tag lines are coded properly (i.e., data bytes can be transferred only when tag lines are 00).



SK0 = SEEK TRACK 0
DR = FLEXIBLE DISK DRIVE
MC = MASTER CLEAR

T.O. = TIME OUT
ALL TIMES MAXIMUM UNLESS NOTED OTHERWISE.

NOTE 1: The READY line will indicate the READY condition of Drive #1, Module A.

Figure 4-2. Master Clear Timing

4.2.3 DATA ENABLE

Data Enable active to the Adapter indicates:

1. Data and tag lines are stable and information (track address, sector address, function code or data byte) is available to the Adapter.

2. Request for Adapter to put data byte or status code on lines.

The leading edge of Data Enable indicates that tag and data lines are stable. Data Enable is required for the transfer of any information (track address, sector address, function code, data byte, or status code) between the Host and Adapter. One byte of information is transferred with each Data Enable. Data Enable will normally be reset by Host when the Adapter activates the Data Strobe line.

If the Adapter does not respond with Data Strobe the Host System is permitted to drop Data Enable after one second. This is not the normal Data Enable/Data Strobe Timing.

NOTE

Data Enable should not be set and reset inadvertently since the setting of Data Enable is remembered by the FDDS and when recognized the tag line state may be meaningless, but the FDDS does not know this and will execute according to its interpretation of the tag lines.

4.2.4 DATA STROBE

A Data Strobe signal from the Adapter will acknowledge Data Enable from the host system and indicates that the Adapter will perform as follows:

1. During decode track, strobes in the track address.

2. During decode sector, strobes in sector address.

3. During the write mode, strobes write data from the host system into buffer.

4. During the read mode, strobes out data from buffer to host system.

5. During decode function, strobes in the data for the function.

   (Data Strobe returned for function after validity of function verified. Will be returned for valid or error function.)

6. During Status Request, strobes out status code to host system.
7. During Set Mode, strobes in Mode Code.

Data Strobe is activated in response to each Data Enable from the Host during the transfer of information. One byte of information is transferred to or from the Adapter with each Data Strobe. Data Strobe is reset by the Adapter when the Host deactivates Data Enable. See Figure 4-1 for Timing Sequence Diagram.

4.2.5 BUSY AND INTERRUPT

The Adapter will activate both the Busy and Interrupt lines to indicate an error condition (Write Fault, CRC Error, Access Error, Buffer Overload/Underload, or Illegal Code Received, Transfer Timing Error, or Format Track Over/Underflow). When an error condition occurs, the Adapter logic will ensure that Busy is set at least 1 us before Interrupt is activated. Only a Status Request command or Master Clear from the Host will clear both the Busy and Interrupt lines.

If a Restore function is issued to a selected drive and there is no return signal from that drive, (i.e., the head does not reach track 00 within .8 sec) the Adapter will activate both Busy and Interrupt to indicate an error condition (Access Error).

Busy and Interrupt will also be activated during any read or write function when Request for Data Transfer (RDT) status occurs (see section 4.2.10.7) and the Interrupt due to RDT has been enabled by a bit in the function code. In this case a Status Request Command will only clear the Interrupt line and not reset Busy.

The Adapter will activate the Busy line during any control function except Read Buffer, Write Buffer, Status Request, Set Mode and Module Select. (Refer to Paragraph 4.2.9 for control functions.) An error-free Operation Complete will clear the Busy signal at least 1 us before Interrupt is set.

When an Interrupt is activated the Host must issue a Status Request to the selected drive to clear Interrupt.

4.2.6 BUSY

The Busy line is set while executing all control functions to a disk drive (except Read Buffer, Write Buffer, Status Request, Set Mode and Module Select) and remains set if an error condition occurs. The Busy line is also set during a Master Clear until the read/write heads in all drives are restored to track 00 or Master Clear timeout is complete, at which time Busy is reset. Busy inhibits all functions except Status Request from being accepted unless it has been set for an error condition. If a function other than Status Request is commanded while Busy is active (during a legal function), the original function will not be affected. There will be no response to the second function.

4.2.7 INTERRUPT

The Interrupt line is set whenever any of the following conditions occur: Operation Complete, RDT (if bit seven set), Write Fault, CRC Error, Access Error, Buffer Overload/Underload, Illegal Code Received, Transfer Timing error and Format Over/Underflow. The Request for Data Transfer Interrupt may be enabled by setting bit seven in the function code in any read or write disk function except for format (Busy status bit being set with Deleted/Defective Record does not cause an error Interrupt to be set). The Not Ready status or Idle does not cause Interrupt.

4.2.8 READY

Adapter will monitor the ready condition of each drive. The Adapter will transmit a multiplexed Ready Signal to indicate that the selected drive is detecting index pulses at proper speed (360 r/min ±4.0%). Speed tolerance is checked during Adapter idle condition on the last selected drive or Drive #1 of Module A following a Master Clear.

The individual drive ready signals will be latched when in their "Not Ready" condition. These latches will be cleared only after a Status Request for that drive or Master Clear. Thus the "Not Ready" history of a drive is remembered even though the drive is not selected.

4.2.9 FUNCTION CONTROL

Function control was introduced in Section 3.11.9. The functions listed in Table 3.2 are described in detail in paragraphs 4.2.9.1 through 4.2.9.12. Timing is shown in Figure 4-1. The Host activates Tag 1 and Tag 2 and the Data Lines followed by DATA ENABLE when Tag lines and Data lines are stable. The FDA raises Data Strobe after it has strobed a function into its internal latch during Data Enable.

4.2.9.1 Module Select (M001 0100)

The subsystem may be configured with up to four drives and the drives are partitioned in pairs referenced as Module A and Module B. Module A is selected by transferring a module select function where Bit M = 0 and Module B is selected if Bit M = 1. Once a module has been selected that module will remain selected until another module select function is received. All disk functions assume the selected module, except for status request which specifies module and drive, but does not redefine module or drive selection.

4.2.9.2 Drive/Head Selection

Drive Selection

A Drive Selection is required for all functions except Read Buffer and Write Buffer. Depending on the condition of bit 8 in the control function code, Drive #1 or #2 will be selected. If bit 8 is 0, #1 is selected. If bit 8 is 1, #2 is selected. The selected drive will be remembered until a new disk function (not including Read Buffer, Write Buffer, Status Request, Module Select or Set Mode) is commanded by the Host or a Master Clear resets to Drive #1, Module A. A status request for a non-selected drive will not change drive selection. Following a Module Select function, the drive selected from a previous Function Select will remain unchanged, only the module assignment will be new.

Head Selection

A head selection is required for all functions except Read Buffer, Write Buffer, Module Select, Set Mode and Status Request.

The most significant bit of the sector address byte transferred by the host determines the head selection. If the bit is a zero, head zero is selected, and if a one, head one is selected. Note that if a 9404 single sided drive is installed this bit must be zero. If a two-sided 9406 drive is installed the bit may be a zero or a one.

4.2.9.3 Drive Head Loading/Unloading

Head loading of the read/write head in each drive will be performed by the Adapter. When the Host issues a function requiring head load (Read Disk, Write Deleted Record, Write Disk, or Format). The Adapter logic will automatically load the head of the selected drive, complete the function, and unload the head after four index pulses have been detected (if no new command is received).

4.2.9.3.1 Access Time

Access time includes move time plus head-load-and-settle time plus latency time. The access time is as follows:

MOVE TIME + HD LD & SETTLE + LATENCY = ACCESS TIME

9404:				
Maximum	770 ms	*60 ms	173 ms	943 ms
Average	260 ms	*60 ms	83 ms	343 ms
Minimum	20 ms	*60 ms	0 ms	60 ms
9406:				
Maximum	248 ms	*60 ms	173 ms	421 ms
Average	96 ms	*60 ms	83 ms	179 ms
Minimum	23 ms	*60 ms	0 ms	60 ms

4.2.9.4 Set Mode (0001 1000)

When the host issues a Set Mode Function, the Adapter will accept the next data transfer byte as the Mode Code. The Mode Code is utilized to specify to the Adapter the characteristics of the media being utilized (i.e., Double or Single Bit Density and Buffer size required.)

These characteristics are required to establish the proper read/write mechanism to the Selected Drive and to define buffer size characteristics for Buffer over/under flow diagnosing. (See 4.2.10.11).

MODE CODE

Bit	8	7	6	5	4	3	2	1
	B	D	X	X	X	X	X	X

B Denotes Buffer Size

0 = 128 Bytes
1 = 256 Bytes

D Denotes Density

0 = Double Density
1 = Single Density

More details about double density and single density recording are given in section 4.5.

*This time is overlapped with the Move Time. On consecutive commands (within four index pulses) the head will remain loaded and this time will not be a part of Access Time.

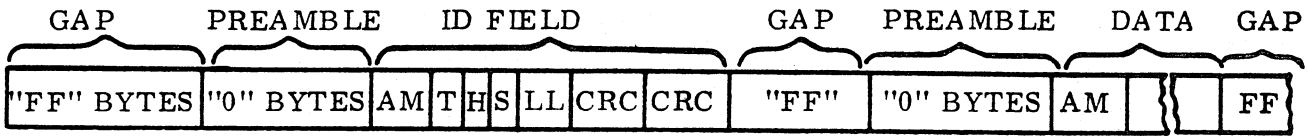
4.2.9.5 Format Media (D001 0001)

The Function code D001 0001 means that the Host wants to give information to Adapter on formatting of the media. The Host first transfers the needed information for formatting the media using a Write Buffer Function and then issues a Format Media Function to begin the actual formatting procedure.

Some aspects of the media format are dictated by hardware design and cannot be changed. The Format Media Function merely tells the Adapter to insert certain information within the established formatting framework. The details as to what this framework looks like are given in this section for those areas which can be affected by the Format Media function and in section 4.5 for those areas which affect data recovery theory of operation.

4.2.9.5.1 Address Field

The address field is formatted according to the following diagram:



The seven (7) 8-bit bytes of the address field shown above are described as follows:

1. AM - This is the Address Mark which is a unique character defining the start of an address field. See Section 4.6.3.
2. T - This is the Logical Track Number of the Logical Track which contains this address field. T is equal to the physical track number, except when bad tracks are formatted (see 4.9.5.1(7.)) then T may be 1 or 2 less than physical track number.
3. H - 00_H for 9404 FDD
   H - 00_H for 9406 FDD side 0
   H - 01_H for 9406 FDD side 1
4. S - This is the sector number of the sector belonging to this address field. It will be a number from 1 up to the maximum number of sectors on the particular track. The maximum number of sectors is a function of the byte "LL" (following S) and the density of the recording.
5. LL - This byte is a code which informs the Adapter of the maximum number of sectors on the particular track. Table 4-1 shows meaning of the "LL" code in terms of maximum sectors per track for single and double density and the corresponding number of bytes per data field.

Table 4-1.
Maximum Sectors Per Track for Single and Double Density

LL_{HEX}	SINGLE	DOUBLE	NUMBER OF DATA BYTES/ DATA FIELD
00	26	Not Applicable	128
01	15	26	256
02	8	15	512
03	4	8	1024
04	2	4	2048
05	1	2	4096

6. CRC - These two bytes are Cyclic Redundancy codes for verification of a valid header read.
7. Bad Tracks - In the case of a bad track the address field is as shown below:

At most two tracks may be flagged as bad tracks.

4.2.9.5.2 Sequence of Operations for Formatting Media

When the host wishes to format a media the following sequence of operations is required:

1. Issue a Write Buffer Function.

2. Transfer the following sequence of data to the adapter buffer.

   a. Byte #1 - Track 0 Density

      00_{hex} = Single Density

      01_{hex} = Double Density

   b. Byte #2 - Track 1-76 Density

      00_{hex} = Single Density

      01_{hex} = Double Density

   c. Byte #3 - LL for the address fields on Track 0.

   d. Byte #4 - LL for the address fields on Tracks 1-76.

   e. Bytes 5 through (4+N)* - Sequence of sector numbers to be recorded on Track 0. The variable sequence of sector numbers is allowed to provide for interlacing sectors.

      NOTE

      *N is defined by the number of sectors on the track. (see Max. Sectors per Track (see Table 4-1).

      Byte X, where $5 \leq X \leq 4 + N$, contains the logical sector number to be formatted at physical sector X-4.

   f. Bytes (5 + N) through (4 + N + M) - Sequence of Sector numbers to be recorded on tracks 1-76. (see e. above) where M is defined by the number of sectors per track.

   g. Bytes (5 + N + M) and (6 + N + M) - Physical track numbers to be recorded as bad tracks. If no bad tracks are to be recorded, then these bytes must both be 00_{hex}. If only one bad track is to be recorded then byte (5 + N + M) must contain this physical track number and byte (6 + N + M) must be 00_{hex}.

      EXAMPLE: Assume Track 0 is to be formatted at single density with sector length of 128 bytes and sectors numbered 1-26, consecutively. Assume tracks 1-76 are to be formatted at double density with sector length of 512 bytes and sectors numbered allowing one sector between consecutive logical sector numbers and no bad tracks. The write buffer would be as follows:

BYTE #	$CODE_{HEX}$		
1	00	Track 0 SD	
2	01	Tracks 1-76 DD	
3	00	128 byte sectors Track 0	
4	02	512 byte sectors tracks 1-76	
		PHYSICAL SECTOR #	
5	01	1	
6	02	2	
7	03	3	Order of Sectors on Track 0
.	.	.	
.	.	.	
.	.	.	
30	1A	26	
31	01	1	
32	09	2	
33	02	3	
34	0A	4	
35	03	5	
36	0B	6	Order of Sectors on Tracks 1-76
37	04	7	
.	.	.	
.	.	.	
.	.	.	
43	07	13	
44	0F	14	
45	08	15	
46	00		
47	00	No Bad Tracks	

3. The host issues a track address byte for track zero and a sector address byte for sector one with the most significant bit of the sector address defining head selection (paragraph 4.2.9.2).

4. Host issues the format function to initiate the format of the media. The adapter will set busy and when formatting is completed the adapter will reset busy, set interrupt and provide an operation complete status. The adapter will write only the header information and supply gap for the data fields.

5. The host will write the data fields with its desired data by employing normal disk write functions (see 4.2.9.7) and thus verify the format write.

6. The host will read the data fields by employing normal disk read functions (see 4.2.9.8) and thus verify the write of data fields.

Notice that Track 0 format and density is allowed to be distinct from the format and density of tracks 1-76. This capability is provided to allow the host to define a known format and density for all track 0's and thus when a new media is inserted in a drive the host can read track 0 and use data recorded there to define necessary characteristics of tracks 1-76, such as, density and sector length.

4.2.9.6 Restore (D000 0000)

The Restore command will cause the Adapter to initiate a track 00 seek. No data is transferred during this operation. A Restore should be issued if an Access Error occurs. Upon successful completion of the Restore function, the Adapter sets the Operation Complete status bit and activates the Interrupt. Time out, without Operation Complete, will set the Access error bit in the Status Register.

NOTE

It is imperative that NO data transfer type operation take place concurrently with a Restore Function.

4.2.9.7 Write Disk (DS00 0001)*

The Write Disk command will cause the data in the Adapter's buffer to be written onto the disk in the specified sector of the selected drive. Prior to issuing the Write Disk command, the Full 128 bytes of data must be in the Adapter's buffer for 128 byte sector length or a full 256 bytes of data for sector lengths $\geq$256 bytes.

The sequence of events is as follows: After the track and sector address have been stored and write disk is received, the Adapter activates Busy, loads the head and initiates a track seek and sector search of the selected drive. A minimum 60 milliseconds will be allowed for Head Loading unless head is already loaded; this period will be overlapped with the Access operation. (Refer to Appendix A for timing information and Section 4.7 for more details of the write operation.

The desired and stored track addresses are compared, and the required Step In or Step Out signals are issued to the drive. When the proper track location is reached, the Adapter delays 10 milliseconds before searching for the clock sync preamble, and Address Mark preceding the address field of the desired sector (see Section 4.6). After Address Mark** is detected, the track and sector addresses are read from the disk. If the track address does not compare with the desired address and the address field CRC is valid, the Adapter compensates as discussed in Paragraph 4.2.9.7.1. The Adapter verifies the CRC bytes. If the sector address does not compare with the desired address or a CRC error is detected, the search operation continues and the address field and CRC bytes of each sector (on that track) is checked. If the correct sector cannot be located after one full disk revolution, the Access Error status bit is set or the CRC Error status bit is set provided a CRC error was detected on that track and an Interrupt is flagged with Busy still active. If the sector address does compare and the CRC bytes are valid, the search operation is terminated.

---

*S Denotes whether RDT bit is set.

**See Section 4.6.3 for details.

When the search operation is terminated, the Adapter begins the actual write operation. Write Enable is activated, and data is transferred to the drive to write the preamble bytes of the data field, the Address Mark, number of data bytes specified in the sector header, two CRC bytes (generated by the Adapter), and the first eight '1' bits of the data gap in accordance with the disk format. When this write operation is completed, Busy is deactivated, the Operation Complete status bit is set, and an Interrupt is flagged a minimum of one usec after Busy is reset. Additionally, if bit 7 of the Write Disk command was set, the Request for Data Transfer status bit is set as the Address Mark is transferred to the drive and an Interrupt is flagged.

NOTE

If Write Disk is issued when the buffer is empty or only partially filled or upon detecting the number of data bytes defined by the sector header to be ≥ 256, with the buffer size specified as 128 bytes, the Adapter sets the Buffer Overload/Underload status bit, activates the Interrupt line and holds Busy active.

If several sectors are to be written consecutively, or if the sector length is > 256 bytes, the following mode of operation must be employed. The Host must transfer data to the Adapter's buffer as the Adapter transfers data from the buffer to be written onto the disk. For consecutive sector write the next sector's data (up to 256 bytes) must be in the buffer before the next sector is ready to be written.

The Host can optionally update track and sector information and reissue the Write Disk function. If the track and sector information is not updated the present track is used with the last sector plus one becoming the next sector address. The operation may be repeated for any required number of sectors within a track. When the Adapter has written the specified number of data bytes and the two CRC bytes onto the disk, Busy is deactivated, the Operation Complete status bit is set, and an Interrupt is flagged (as in normal operation).

4.2.9.7.1 Bad Track Compensation

During a track seek operation, if the track address read from the disk does not compare with the stored (desired) address, the Adapter compensates to locate to the proper track. A Step In or Step Out is issued, depending on previous direction, and the new track address is read. If this address does not compare, another Step is issued. If after two compensation steps the actual and stored addresses do not agree at the track location, the Access Error status bit is set and an Interrupt is flagged. The track address may not compare because is was changed to mark a bad track (address = FF) or because it was not the desired address, although valid.

4.2.9.8 Read Disk (DS00 0010)*

The Read Disk command will cause the data at the specified track and sector location on the disk to be transferred to the Adapter's buffer. The track seek and sector search operation is identical to that of a Write Disk command (described in Paragraph 4.2.9.7).

When the desired sector location has been found and the Address Mark preceding the data field has been detected (see Section 4.6.3), the Adapter sets the Request for Data Transfer status bit and activates the Interrupt line if bit 7 of the Read Disk Command was set. The Adapter then transfers the data from the disk to the buffer. If the sector size is > 256 bytes, the Host must empty the buffer in order to provide space for additional data bytes, otherwise a transfer timing error will occur. CRC bytes are checked and, if in error, the CRC Error status bit is set, and an Interrupt is flagged (with Busy still active). If the CRC bytes are correct, Busy is deactivated, the Operation Complete status bit is set and an Interrupt is flagged. In either case, if the Address Mark was detected as a deleted/defective record code, the Deleted/Defective Record status bit is set.

NOTE

If Read Disk is issued when the buffer is full or partially full, a Buffer Overload/Underload status is set, Busy remains activated and an Interrupt is flagged (but the original data will remain in the buffer).

If several sectors are to be read consecutively or if the sector length is > 256 bytes, the following mode of operation must be employed. The Host transfers data from the adapter's buffer as the adapter transfers data to the buffer from the disk. For consecutive sector read the buffer must be empty before the next sector is ready to be read. The Host can optionally update track and sector information and reissue the Read Disk Function. If the track and sector information is not updated the present track is used with the last sector plus one becoming the new sector address. This operation may be repeated for any required number of sectors within a track. When the adapter has read the specified number of data bytes and the two CRC bytes read and validated, Busy is deactivated, the Operation Complete Status bit is set, and an Interrupt is Flagged (as in normal operation).

---

*S Denotes whether RDT Bit is set.

4.2.9.9 Read Buffer (0010 0000)

The Read Buffer command will allow a specified number of bytes (i.e., Buffer size defined by set mode) of data in the Adapter's buffer to be transferred to the Host. The Host transmits the Read Buffer command and activates Data Enable to indicate that the Adapter may activate the data lines. The Adapter places the first byte of data on the data lines and activates Data Strobe, indicating that the data is present. The Host receives the data and terminates Data Enable which in turn terminates Data Strobe. (Refer to Appendix A for timing information.) The Data Enable and Data Strobe exchange continues for each byte of data until the entire Host specified number of bytes have been transferred. The Host system must ensure that all bytes have been transferred and terminate the Read Buffer operation. The Adapter does not flag a Busy or Interrupt during this operation.

When the Host completes reading the buffer, the Adapter does not set Operation Complete and remains in Idle status.

NOTE

If an attempt is made to transfer data from the buffer when it is empty, the Adapter will not respond to Data Enable with Data Strobe and no Data will be transferred.

4.2.9.10 Write Deleted Record (DS00 0100)

This command will cause a Write Disk function to be performed, but the Address Mark preceding the data will be changed to flag the sector as a deleted/defective record. (Refer to Paragraph 4.2.9.7 for Write Disk description.)

If several deleted or defective sectors are to be written continuously, the optional mode of operation discussed in Paragraph 4.2.9.7 may be employed.

4.2.9.11 Write Buffer (0000 1000)

The Write Buffer command will allow a specified number of bytes, (i.e., Buffer Size defined by Set Mode) of data to be transferred to the Adapter's buffer from the Host. After transmitting the Write Buffer command, the Host places a data byte on the data lines with "00" tag and activates Data Enable to indicate to the Adapter that data is present. The Adapter strobes the data into its buffer and activates Data Strobe to indicate to the Host that the data was received.

The Host deactivates the data line and terminates Data Enable, at which time the Adapter terminates Data Strobe. (Refer to Appendix A for Timing Sequence.) The Data Enable and Data Strobe exchange continues until all bytes have been transferred and the buffer is full. The Host system must ensure that all bytes have been transferred and terminate the Data Transfer operation. The Adapter does not flag a Busy or Interrupt during this operation. When the Host completes filling the buffer, the Adapter does not set Operation Complete and remains in Idle status.

NOTE

If an attempt is made to transfer data to the buffer when it is full, the Adapter will not respond to Data Enable with Data Strobe and no Data will be transferred.

4.2.9.12 Status Request (DM01 0000)

The Status Request was described briefly in Section 3.11.2. DATA STROBE, INTERRUPT, READY, and BUSY are transmitted on individual lines, but 13 other status conditions are coded on the data lines (see Table 3-3). Table 4-2 lists the 13 status conditions and the associated binary codes. Timing for the status transfer sequence is shown in Figure 4-1 at the right side of the figure.

When the Adapter is Busy the Host may issue a Status Request at any time to the currently selected drive without affecting any existing operation. When the Adapter is not Busy, the Host may issue a Status Request to any drive. A Status Request will normally be issued upon receiving an Interrupt from the Adapter. If a Status Request is issued to a non-selected drive while the adapter is Busy, there will be no Data Strobe response to Data Enable.

The TAG lines signal a function is on the data lines. DATA ENABLE indicates that the data lines are stable. When the FDA "reads" the data lines it activates DATA STROBE. At this point the data lines are coded to indicate that the Host requests status information. After DATA STROBE is deactivated by the FDA, the Host activates DATA ENABLE with "00" tag indicating to the FDA that the 8 bit status code should be put on the data lines. The FDA puts the status code on the data lines and activates DATA STROBE when the data lines are stable. The Host deactivates the DATA ENABLE line when it has "read" the data lines.

The Adapter contains a Status Byte for each drive. The Status Byte (of the selected drive) is reset when the Status Byte Code is setup for transfer to Host. Status for non-selected drives will reflect only ready/not-ready status.

4.2.10 STATUS INTERPRETATION

When the Host issues a Status Request, the Adapter will respond with status information coded on the data lines. Status conditions are described in Paragraph 4.2.10.1 through 4.2.10.11 below. Status codes are listed in Table 4.2.

Table 4-2. Status Codes

STATUS CODE								STATUS
b8	b7	b6	b5	b4	b3	b2	b1	
0	0	0	0	0	0	0	1	Operation Complete
1	0	0	0	0	0	1	0	Illegal Code Received
0	0	0	0	0	1	0	0	Deleted/Defective Record
1	0	0	0	1	0	0	0	Write Fault/Write Protect
1	0	0	1	0	0	0	0	Cyclic Redundancy Code (CRC) Error
1	0	1	0	0	0	0	0	Access Error
1	1	0	0	0	0	0	0	Request for Data Transfer
1	0	0	0	0	0	0	0	Busy
0	0	0	0	0	0	0	0	Idle
1	0	0	0	0	0	1	1	Buffer Overload/Underload
1	0	0	0	0	1	1	0	Transfer Timing Error
1	0	0	0	1	1	1	0	Format Track Over/Under Flow
1	1	1	1	1	1	1	1	Not Ready
NOTE: Status Bits May Overlap.								

4.2.10.1 Operation Complete (0000 0001)

This status occurs when an operation involving the disk has been completed (i.e., Write Disk, Write Deleted Record, Read Disk, Restore, or Format). For Write/Read data transfer operations involving the disk, the Operation Complete status bit is set after all bytes of data have been transferred between the Adapter and disk, and the two CRC bytes have been written or read. The Operation Complete status bit is set during a Restore operation when track 00 is successfully located.

For format operation the Operation Complete status bit is set following format write of all 77 tracks on the media.

4.2.10.2 Illegal Code Received (1000 0010)

This status is set (before Data Strobe is returned) when a Disk function is commanded if any of the following are true:

1. Any function code not defined in Paragraph 3.11.1 is received.
2. Track address is greater than 76.
3. Sector Address transferred from the Host is not equal to the range defined by Mode Code.

4.2.10.3 Deleted/Defective Record (0000 0100)

This status occurs when the Address Mark of the addressed sector is checked during a Read Disk operation and detected to indicate a deleted/defective record. The Deleted Record status will be set and no Interrupt will be transmitted; however, the operation will continue until completed, at which time operation complete interrupt occurs.

4.2.10.4 Write Fault/Write Protect (1000 1000)

This status occurs when the Write Fault signal is received from the selected drive or if the media is write protected and a write operation is attempted.

4.2.10.5 CRC Error (1001 0000)

This status occurs when the CRC detected on the address field during a read or write operation is incorrect, or when the CRC detected on the data field during a read operation is incorrect. Activation of this status bit for the address field results in the operation to be aborted. Activation of this status bit for the data field results in the Operation Complete status bit being set (and both Busy and Operation Complete are set; whereas in error-free operation, Busy is reset when Operation Complete is set).

4.2.10.6 Access Error (1010 0000)

This status occurs when the desired track cannot be located, as discussed in Paragraph 4.2.9.7.1 (Bad Track Compensation) or when the desired sector cannot be located within one full disk revolution, as discussed in Paragraph 4.2.9.8 or if the Address Mark preceding the desired data field has not been detected within approximately 2 milliseconds after the correct address field has been processed. This status also occurs during a Restore when the selected drive has not responded within a pre-determined time (see Paragraph 4.2.9.6).

4.2.10.7 Request for Data Transfer (1100 0000)

This status occurs when the seek operation is complete and the Address Mark preceding the Data is detected or written, if bit 7 of the function code (which enabled this status) was set.

4.2.10.8 Busy (1000 0000)

This status occurs any time the adapter is executing a disk function or an error was detected.

4.2.10.9 Idle (0000 0000)

This status occurs any time the Adapter is idle (not communicating with any drive).

4.2.10.10 Not Ready (1111 1111)

This status occurs whenever the selected drive is not ready for operation as defined in Paragraph 4.2.8 (Ready line). This status will not cause an Interrupt.

The individual drive ready signals will be latched when in their "not ready" condition. These latches will be cleared only after a Status Request for that drive or Master Clear. Thus the "Not Ready" history of a drive is remembered even though the drive is not selected.

4.2.10.11 Buffer Overload/Underload (1000 0011)

This status occurs if an attempt is made to transfer data from the buffer to the disk (Write Disk or Write Deleted Record) when the buffer has not been filled with exactly the number of bytes specified by Set Mode, or if an attempt is made to transfer data from the disk to the buffer (Read Disk) when the buffer is full or partially full, where full is defined by Set Mode (see Section 4.2.9.4).

4.2.10.12 Transfer Timing Error (1000 0110)

When reading or writing the disk if the amount of data to be transferred is greater than 256 bytes, then the adapter uses its buffer in the wrap-around mode, thus the host must transfer data at the rate being written or read. If the host falls behind more than 256 bytes then a transfer timing error will occur.

4.2.10.13 Format Track Over/Under Flow (1000 1110)

When the adapter is executing a FORMAT function, it will commence writing at the index-hole. If a second index-hole is detected before the adapter has completed the track write this constitutes an overflow and a Format Track Over/Under Flow status will be indicated. If the second index pulse has not occurred when the track formatting write is complete the firmware monitors the time until the second index pulse occurs. If the time exceeds an interval dictated by a firmware delay loop, this constitutes an underflow and the Format Track Over/Under Flow status is indicated.

4.3 INTERFACE CIRCUIT AND INTERFACE CONTROL

This includes the logic required to interface the FDA to the Host and the Flexible Disk Device (FDD). Programmable Peripheral Interface (PPI) devices are used as the basis for the I/O control system. Use of these devices expands the number of I/O ports available from the 8080 Microprocessor and also releases it from the undesired timing constraints that would be imposed on it by the circuits requiring service by the 8080. See sheet 6 of Figure 5-4 and sheet 11 of Figure 5-5. Refer also to the block diagrams, Figures 4-6 and 4-7. See Section 4.10 for details on the 8080 Microprocessor system operation.

4.3.1 HOST/FDA INTERFACE

PPI #1 is programmed as the Host/FDA bi-directional data port. The basic transfer of data is accomplished with a handshaking sequence between Data Enable and Data Strobe. A Data Enable from the host sets an interrupt flip-flop (5D, M.P.2 Schematic Figure 5-5, sheet 3). In the process of servicing the interrupt the 8080A will inform DMA CONTROL which enables PPI #1. The completion of this action will set a data strobe flip-flop (5D, M.P.2 Schematic Figure 5-5, sheet 5) which after some control gating, is the data strobe output. This controlled by DMA CONTROL uses the Up/Down counter as its basis for control of the data strobe. See Figure 4-3.

The Up/Down counter control is required so that when the buffer is being filled by the Host and emptied by the DMA the Host must not be allowed to enter a byte before a memory location is available. A special Up/Down counter (5G and 5F, M.P.2, Sheet 9, Figure 5-5) circuit thus will maintain the balance of data within the buffer. This is shown by HOST PORT which goes active at the counter borrow or carry and inactive when the counter counts. The same action occurs in reverse when the DMA is filling the buffer. The Host must not take a byte before the DMA has entered that byte. See Figure 4-3 and 4-4.

PPI #1 Port C controls bi-directional data flow. Port A is bi-directional data bus to Host. Port B is parallel data from the selected FDD. The data bus (DB) of PPI #1 inputs Host and FDD data to the 8080A system or memory.

Signal assignments for the three PPI circuits are listed in Table 4-3. Figure 4-7 shows a block diagram of a PPI, type 8255, together with basic operation table. Detailed operation can be found in the vendor literature on the 8080 system.

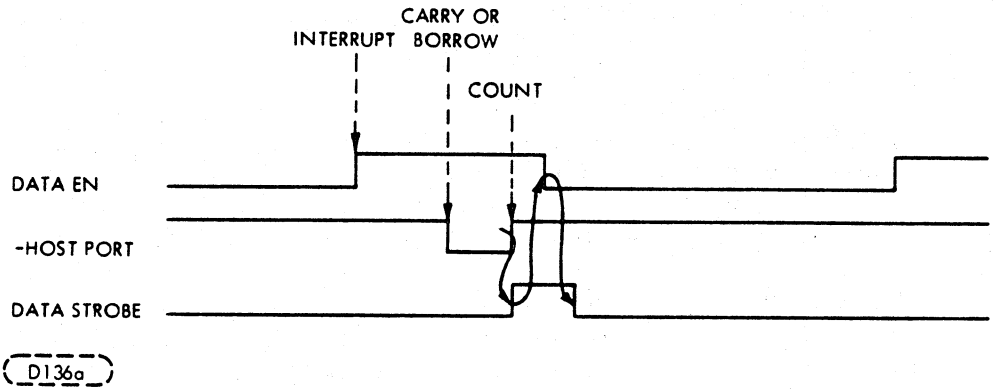


Figure 4-3. HOST Interface Data Transfer Timing

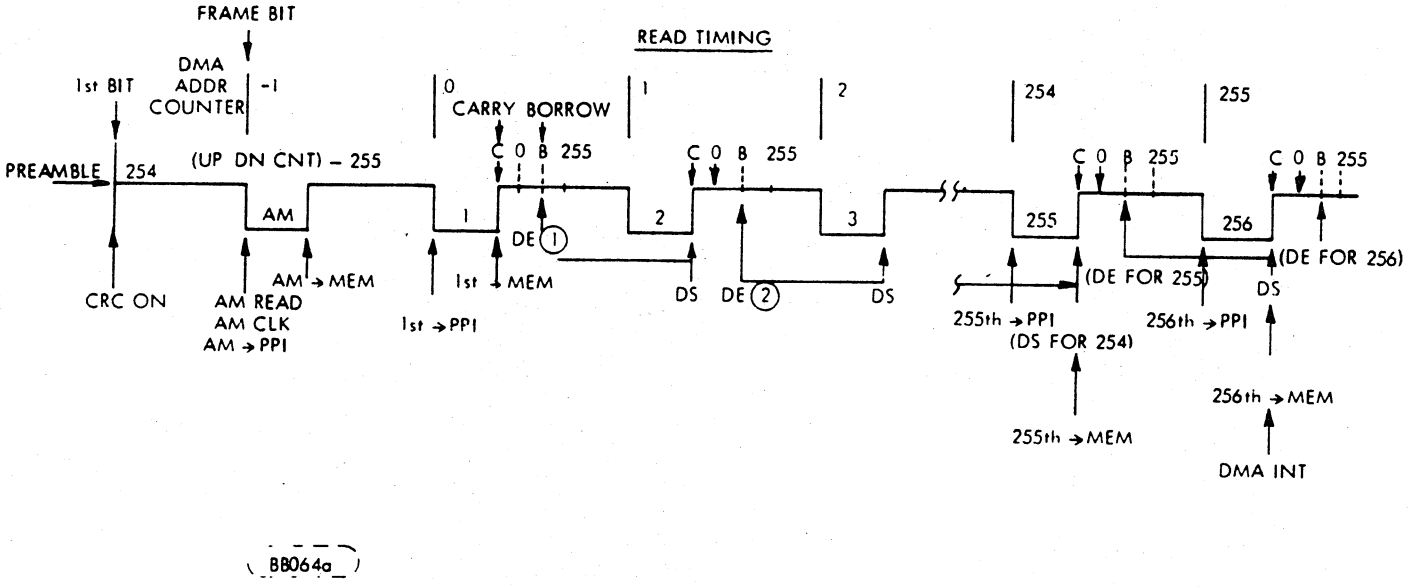


Figure 4-4. Up/Down Counter Control of Data Strobe for a Read

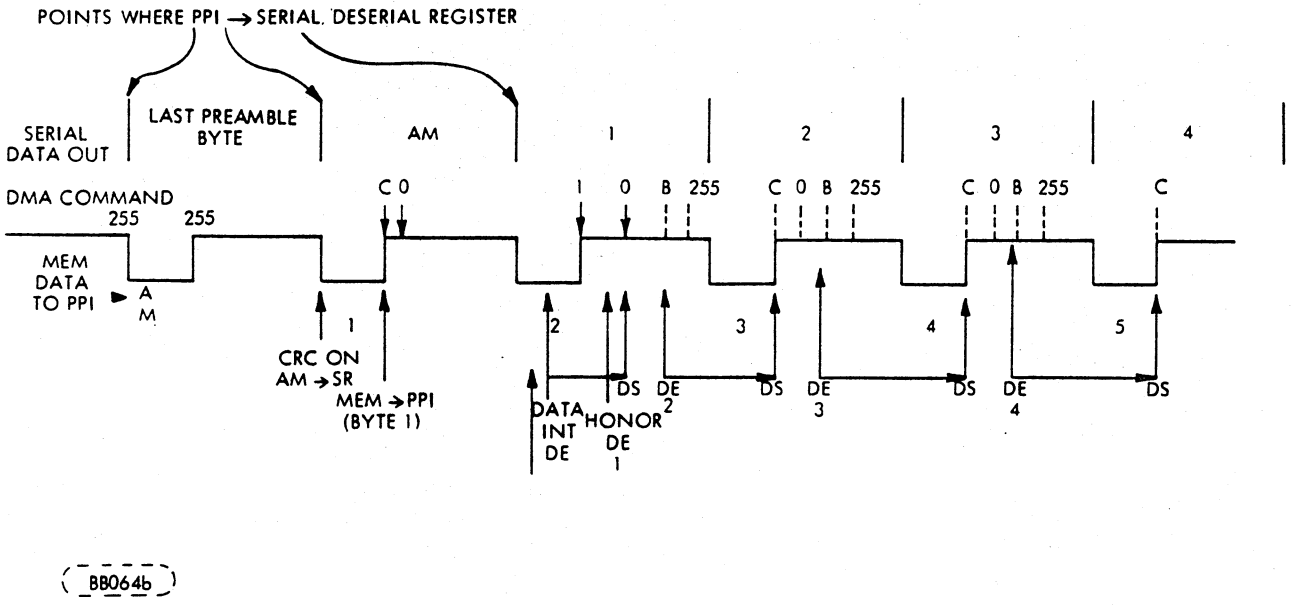


Figure 4-5. Up/Down Counter Control of Data Strobe for a Write

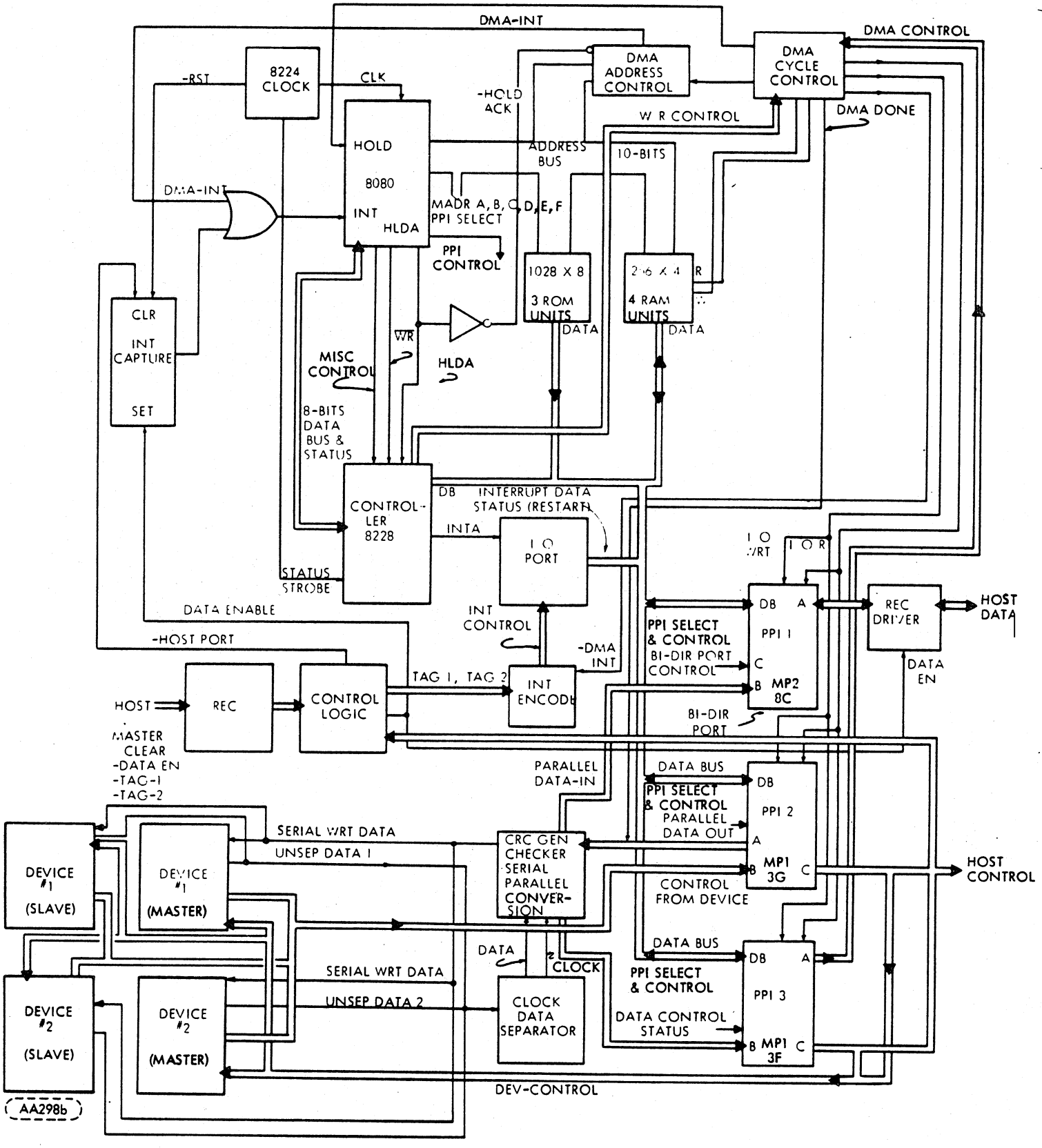


Figure 4-6. FDA Block Diagram

4.3.2 FDA/FDD INTERFACE

PPI #2 and PPI #3 interface the FDA and the two FDD units.

PPI #2 - Port B is programmed as an input port from FDD #1 and #2 from both master and slave. Port C is an output port to reset the Ready latches and control data recovery circuits. Port A is the parallel data port to the serial/de-serializer circuit. Port A transfers parallel data to be written on the FDD.

PPI #3 - Port A is an output port which selects FDD, Head, and data recording method. Port B is an input port from the data recovery circuits. These input lines include correct CRC indication, address mark read, etc.

Port C is an output port which includes output leads to the FDDS and to the host.

Table 4-3. PPI Signal Assignments

PPI 1-A	
PA0 DATA0 T/F HOST PA1 DATA1 T/F HOST PA2 DATA2 T/F HOST PA3 DATA3 T/F HOST PA4 DATA4 T/F HOST PA5 DATA5 T/F HOST PA6 DATA6 T/F HOST PA7 DATA7 T/F HOST	Bi-Directional Data to and from HOST
PPI 1-B	
PB0 DATA0 FROM SERDES PB1 DATA1 FROM SERDES PB2 DATA2 FROM SERDES PB3 DATA3 FROM SERDES PB4 DATA4 FROM SERDES PB5 DATA5 FROM SERDES PB6 DATA6 FROM SERDES PB7 DATA7 FROM SERDES	Parallel Data received from Device (Converted from Serial Input)
PPI 1-C	
PC0 NC PC1 NC PC2 SERDES DATA STROBE PC3 NC PC4 Enable Host Data (in) PC5 NC PC6 Enable Host Data (out) PC7 NC	Control lines which control the bi-directional bus port A and S/D Port B

*Serializer-Deserializer

Table 4-3. PPI Signal Assignments (continued)

PPI 1-DB

DB0 DATA 0 T/F M.P. MEMORY
DB1 DATA 1 T/F M.P. MEMORY
DB2 DATA 2 T/F M.P. MEMORY
DB3 DATA 3 T/F M.P. MEMORY
DB4 DATA 4 T/F M.P. MEMORY
DB5 DATA 5 T/F M.P. MEMORY
DB6 DATA 6 T/F M.P. MEMORY
DB7 DATA 7 T/F M.P. MEMORY

} Bi-Directional Data to and from Microprocessor memory

PPI 1 Miscellaneous*

CS/ CHIP SELECT - Enables communication between 8255 and 8080.
RD/ READ INPUT - Enables 8255 to send data or status to 8080.
WR/ WRITE INPUT - Enables 8080 to write data or control to 8255.
A0/PORT ADDRESS
A1/PORT ADDRESS } Controls selection of the three ports or control word reg.
RST/RESET - Clears all internal registers; ports set to input mode

PPI 2-A

PA0 DATA0 TO SERDES
PA1 DATA1 TO SERDES
PA2 DATA2 TO SERDES
PA3 DATA3 TO SERDES
PA4 DATA4 TO SERDES
PA5 DATA5 TO SERDES
PA6 DATA6 TO SERDES
PA7 DATA7 TO SERDES

} Parallel Data Out to Device (Must be converted to Serial Data/CLK)

PPI 2-B

PB0 TRACK 00
PB1 INDEX
PB2 WRITE PROTECT
PB3 WRITE FAULT
PB4 REMOTE READY UNIT 4
PB5 REMOTE READY UNIT 3
PB6 REMOTE READY UNIT 2
PB7 REMOTE READY UNIT 1

} Input lines from FDD Units

*These same signals perform the same functions also on PPI 2 and PPI 3. See also Figure 4-6 for a block diagram of the PPI unit.

Table 4-3. PPI Signal Assignments (continued)

PPI 2-C

PC0 RESET READY LATCH 1
PC1 RESET READY LATCH 2
PC2 RESET READY LATCH 3
PC3 RESET READY LATCH 4
PC4 HOST FILE BUSY
PC5 ENABLE CRC SHIFT
PC6 ID READ
PC7 ENABLE ADDRESS MARK WRT

PPI 2-DB

DB0 DATA 0 T/F M. P. MEMORY
DB1 DATA 1 T/F M. P. MEMORY
DB2 DATA 2 T/F M. P. MEMORY
DB3 DATA 3 T/F M. P. MEMORY
DB4 DATA 4 T/F M. P. MEMORY
DB5 DATA 5 T/F M. P. MEMORY
DB6 DATA 6 T/F M. P. MEMORY
DB7 DATA 7 T/F M. P. MEMORY

} Bi-Directional Data to and from Microprocessor memory

PPI 3-A

PA0 SELECT FDD 1 (MASTER FDD 1)
PA1 SELECT FDD 2 (MASTER FDD 2)
PA2 SELECT FDD 3 (SLAVE FDD 1)
PA3 SELECT FDD 4 (SLAVE FDD 2)
PA4 NOT USED
PA5 HEAD SELECT
PA6 MFM/DF SELECT
PA7 INDEX TO INDEX READ/WRITE ENABLE

PPI 3-B

PB0 -ALL ZEROS
PB1 CRC ON/AM DONE
PB2 NOT USED
PB3 DISK DMA DONE
PB4 INDEX TO INDEX DONE
PB5 HOST DMA DONE
PB6 NOT USED
PB7 DISKETTE TYPE

} Input Control From Data Recovery Circuits

Table 4-3. PPI Signal Assignments (continued)

PPI 3-C	
PC0 -DISABLE TRANSFER TIMING ERROR INTERRUPT	
PC1 HEAD LOAD	
PC2 STEP	
PC3 DIRECTION	
PC4 LOW CURRENT	
PC5 -RD/WRT A	
PC6 WRITE FAULT RESET	
PC7 -EN RD/WRT CNT	
PPI 3-DB	
DB0 DATA 0 T/F M.P. MEMORY	Bi-Directional Data to and from Microprocessor memory
DB1 DATA 1 T/F M.P. MEMORY	
DB2 DATA 2 T/F M.P. MEMORY	
DB3 DATA 3 T/F M.P. MEMORY	
DB4 DATA 4 T/F M.P. MEMORY	
DB5 DATA 5 T/F M.P. MEMORY	
DB6 DATA 6 T/F M.P. MEMORY	
DB7 DATA 7 T/F M.P. MEMORY	

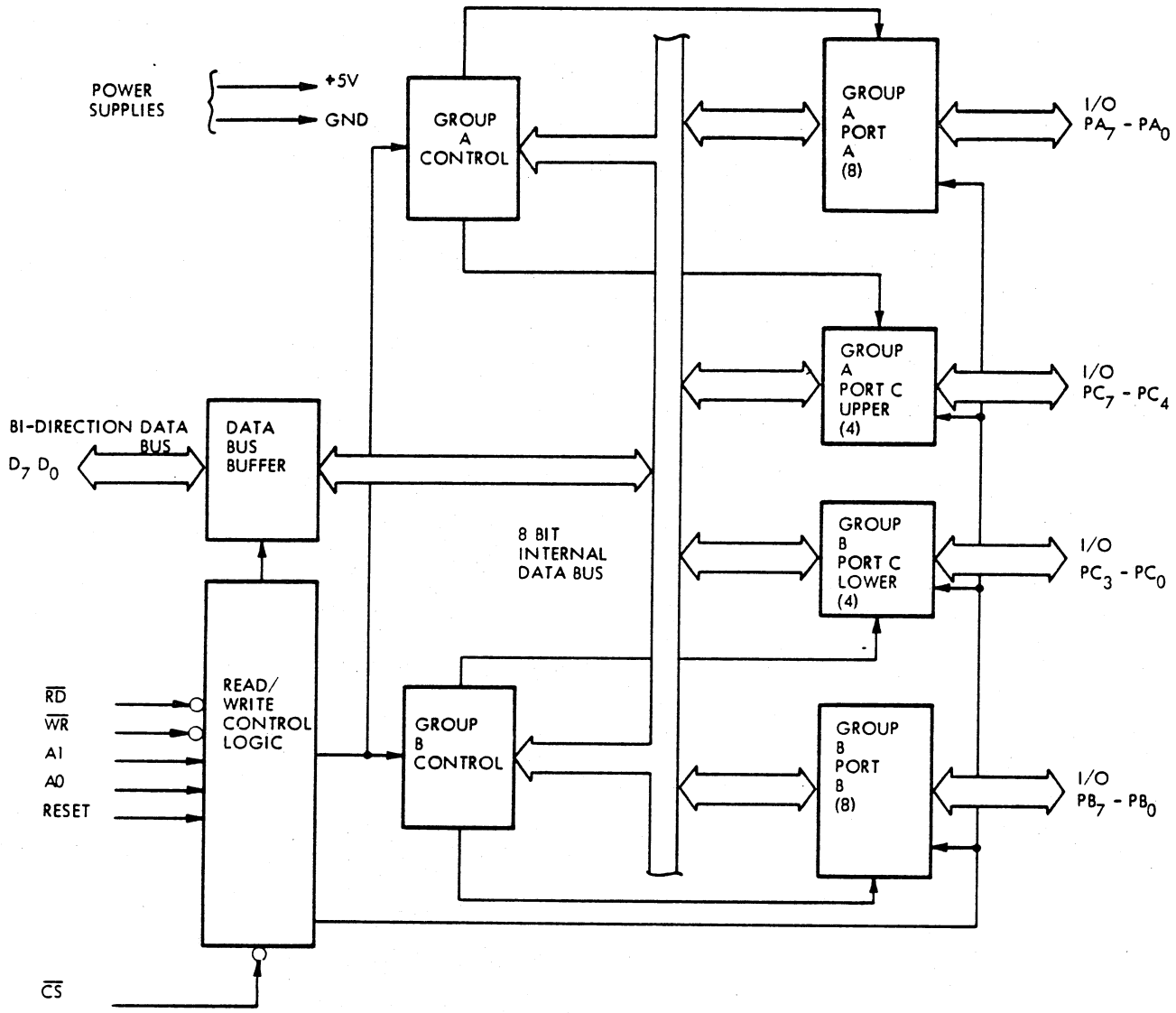
4.4 I/O TIMING SEQUENCES

4.4.1 WRITE CYCLE TIMING

Figure 4-1 illustrates the timing sequence for a single write cycle. The sequence of events is as follows: The Host issues a function code (11) on the tag lines and a Write Buffer Command on the data lines to initiate the write cycle. The tag lines are then coded 00 (Data) and data is transferred on the data lines from the Host to the Adapter's buffer until the 256 byte buffer is full. Handshaking signals (Data Enable and Data Strobe) between Host and Adapter allow for the transfer of each byte of data. The Data Enable line goes true to indicate data is on the data lines; the Adapter acknowledges reception of data with Data Strobe line going true. The leading edge of the Data Strobe signal terminates Data Enable which in turn terminates Data Strobe.

The trailing edge of Data Enable terminates all tag line operational codes and data line signals. These handshaking signals occur when any information (data, track, sector, or function) is exchanged between the Host and the Adapter.

After the data transfer is complete, track (TAG 2, TAG 1 = 01) and sector (TAG 2, TAG 1 = 10) information is transmitted. The function code (TAG 2, TAG 1 = 11) is again transmitted with the Write Disk Command coded on the data lines. This initiates the Write Disk function. The actual function (writing the 256 bytes of data on the disk) is performed at the termination of the function transfer, at which time the Adapter also activates the Busy lines. The Adapter terminates the Busy signal when the operation is successfully completed and activates the Operation Complete status bit and the Interrupt line. The Interrupt is terminated by a Status Request. A typical Write Buffer/Write Disk Timing Sequence is shown in Figure 4-8. A typical Consecutive Sector Read/Write Timing Sequence is shown in Appendix A.



8255 BASIC OPERATION

A1	A0	RD	WR	CS	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION

AA288a

Figure 4-7. Block Diagram of a 8255 PPI Unit

4.4.2 READ CYCLE

Figure 4-9 illustrates the timing sequence for a single read cycle. The read cycle sequence is similar to the write cycle sequence described in Paragraph 4.4.1 following acceptance of Read Disk, the Adapter activates the Busy line and transfers the 256 bytes of data from the disk to the buffer. The Adapter logic terminates the Busy signal when the operation is successfully completed and activates the Operation Complete status bit and the Interrupt line. The Interrupt is terminated by a Status Request.

Upon receiving Operation Complete, the Host transmits the Read Buffer command and activates Data Enable to indicate that the Adapter may activate the data lines. The Adapter places the first byte of data on the data lines and activates Data Strobe, indicating that the data is present.

The Host receives the data and terminates Data Enable which in turn terminates Data Strobe. This Data Enable and Data Strobe exchange continues for each byte of data until the entire 256 bytes have been transferred. The Adapter does not flag a Busy or Interrupt during this operation. When the Host completes reading the buffer, the Adapter remains in Idle status. In all other respects, the read cycle is the same as the write cycle.

4.5 DISKETTE DATA RECORDING TECHNIQUE AND FORMAT

Information is stored on a disc using a code that takes the desired information and converts it to pulses that the recording system can write and recover from the disc. The ideal system requires all the pulses written on the disc be information. The problem with this type of system is when the data is recovered it is not self-clocking. A self-clocking code is Double Frequency (DF) while a non self-clocking system is Modified Frequency Modulation (MFM). The actual flux reversal rate of the two codes are the same; Table 4-4 shows the differences. Both types of recording can be handled by the 9474 FDDS.

Table 4-4.

	DOUBLE FREQUENCY	MODIFIED FREQUENCY MODULATION
Data Bit Density	1836 3268	3672 (outer track) 6536 (inner track)
Data Transfer Rate	249 984 Hz	499 968 Hz
Data Bits/Track	41 664	83 328
Data Bits/Disk Surface	3 208 128	6 416 256
Data Bits/Double-sided Diskette	6 416 256	12 832 512
Cell time	4 µs	2 µs
Max Flux Density (inner track) (Clock and Data)	6536	6536

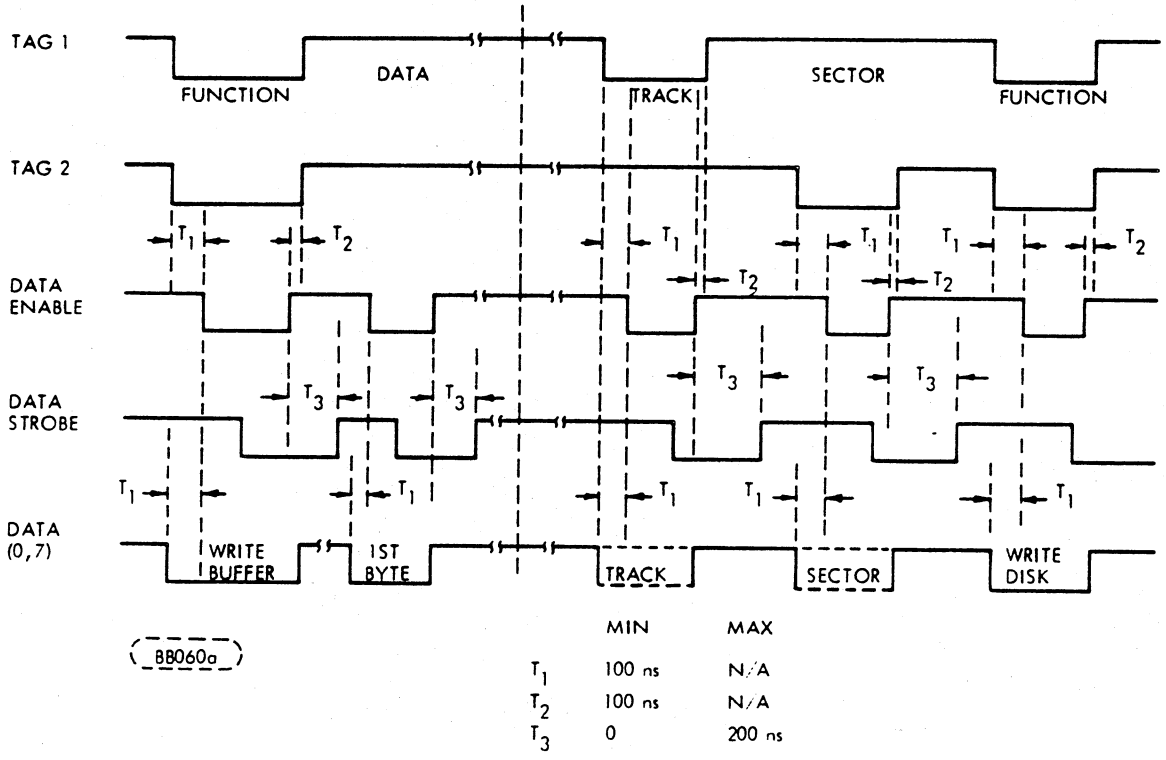


Figure 4-8. Write Buffer/Write Disk a Typical Timing Sequence

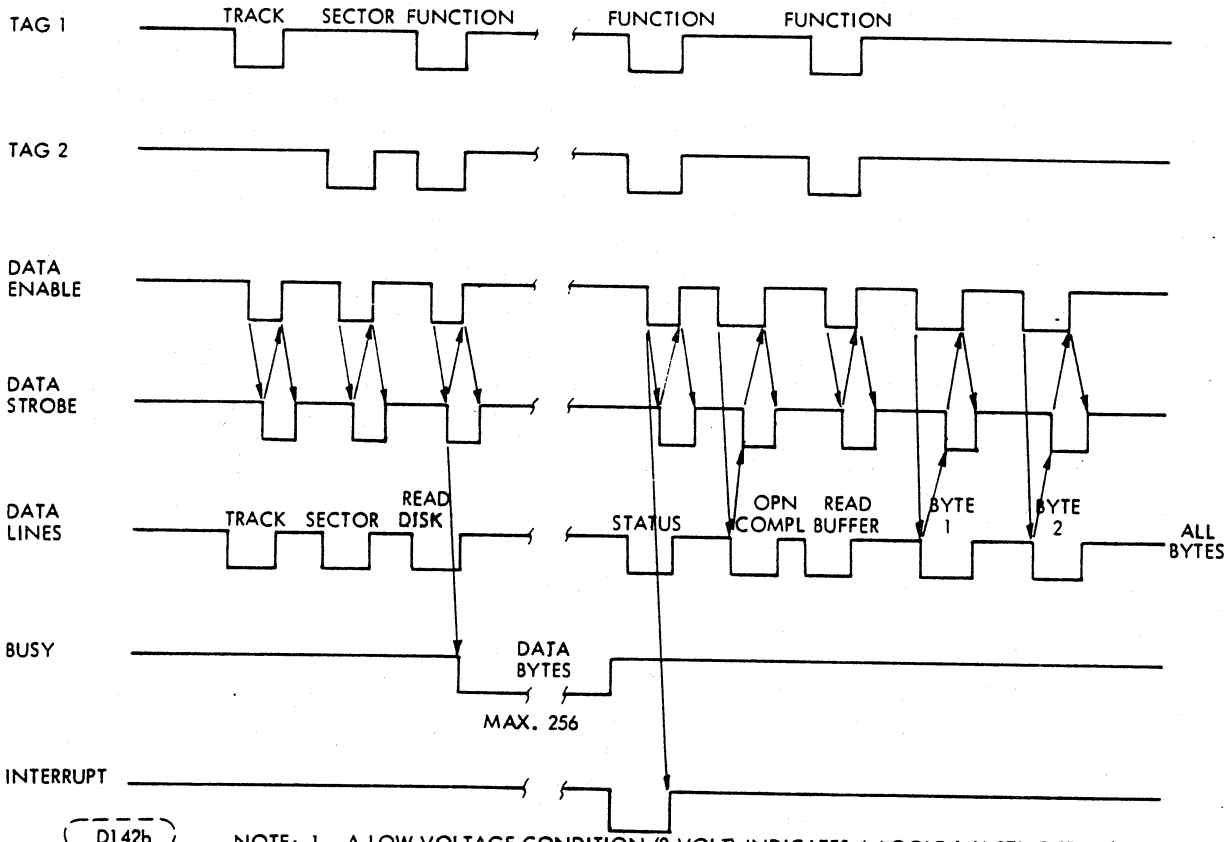


Figure 4-9. Single Read Cycle Timing

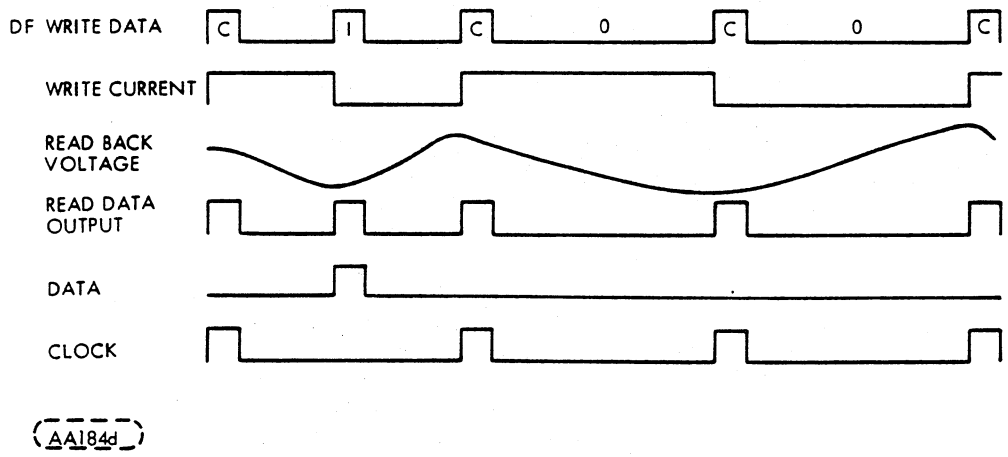


Figure 4-10. Double Frequency

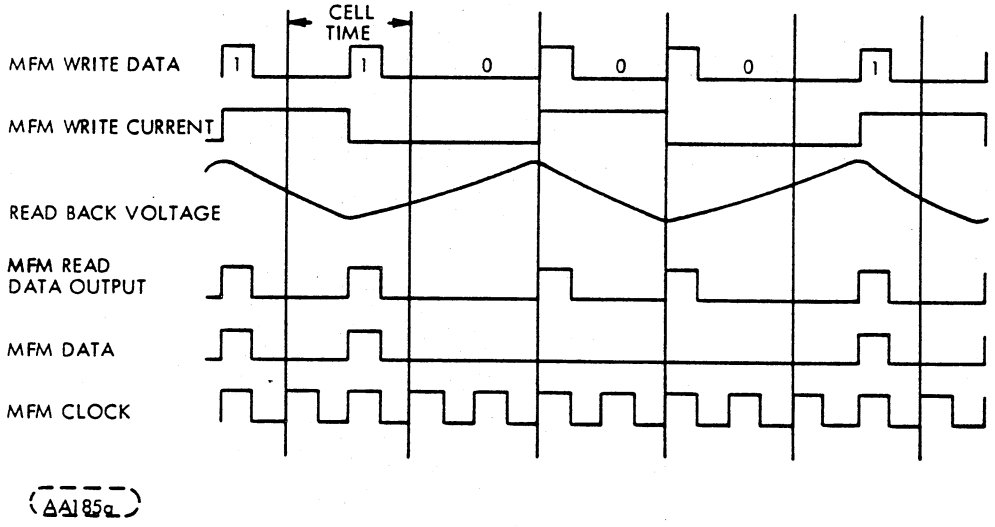


Figure 4-11. MFM Recording

4.5.1 DOUBLE FREQUENCY (DF)

Information is always recorded by inserting clock between each data bit. A "1" bit is defined as a flux transition between clocks while an "0" is defined as the absence of this flux transition. Clocks are always flux transitions (refer to Figure 4-10).

4.5.2 MODIFIED FREQUENCY MODULATION (MFM)

Information is encoded using data and clocks such that the longest time between flux transition is the same as in DF code but clocks are not recorded between data bits (refer to Figure 4-11).

Definition:

1. "1" is defined as a flux transition occurring at the half cell time.

2. "0" is defined as a flux transition occurring at the start of the cell time. A pulse at the beginning of the cell is a clock; however, a clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the preceding cell.

MFM recording requires write compensation to minimize the problem of peak shifting of the pulses.

4.5.3 WRITE COMPENSATION

The write compensation circuit converts the NRZ data into MFM data while compensating for head/media peak shift. Peak shift is an affect that degrades read accuracy by distorting the waveform. Peak shift is the result of the interaction of two adjacent pulses such that the two pulses tend to have a portion of their individual signals superimposed on each other, causing the actual readback voltage to be the algebraic summation of the pulses. Peak shifting occurs when there is a change in frequency such as when bit patterns 011 and 110 are written. Write compensation is applied by writing the pulses 250 ns early or 250 ns late or "on time" when no compensation is needed. More details will be given in Section 4.7 where the Write Function is described in detail. Write compensation is applied only when low current is used for writing MFM data on tracks 42 to 76.

4.6 DATA RECOVERY SYSTEM

The first step in the data recovery process is the creation of a clock which is synced to the Read Clock/Data from the diskette. This is accomplished by circuitry on Microprocessor Number 1, the schematics of which are on sheets 9 and 16 of Figure 5-4. Figure 4-12 shows a simplified logic diagram of the clock generating circuitry from the above two sheets of Figure 5-4, together with timing diagrams for Modified Frequency Modulation (MFM) and Double Frequency (DF) operation of the circuit, also known as a Phase Lock Loop circuit. The operation of the Phase Lock Loop is described in Section 4.6.1. The second step in data recovery is the separation of clock and data from the Read Clock/Data read from the diskette. This is described in Section 4.6.2.

4.6.1 PHASE LOCK LOOP CIRCUIT

The heart of the Phase Lock Loop circuit is a Voltage Controlled Oscillator (VCO) which free runs at 2 MHz. The VCO output is divided by two for "MFM" operation and divided by four for "DF" operation (see Figure 4-12). The divided down signal is compared with a reshaped version of the input Read Clock/Data signal from the FDD. That is, C in the timing diagram is compared with J . If Read Clock/Data leads the VCO signal, a small pulse which is the difference of the two appears at pin 9 of the phase detector (E in Figure 4-12). If the Read Clock/Data lags the VCO signal the difference pulse appears at pin 5 of the detector (D in Figure 4-12). A comparator/amplifier/filter circuit puts out a DC signal whose quiescent value is +3.5 Volts DC, ±.5 Volts (F in Figure 4-12). Pulses on E cause F to go more positive, while pulses on D cause F to go less positive. The frequency of the VCO increase when F goes more positive, and the frequency decreases when F goes less positive. Increasing the frequency of J causes the trailing edges of its pulses to come closer to the trailing edges of the Read Clock/Data pulses when the latter is leading the former. Decreasing the frequency of J causes its trailing edges to drop back to come closer to the trailing edges of C . When pulses C and J coincide the gross frequency adjustment of the VCO stops. However, due to spindle speed variations and other variations in all of the circuitry involved, there is a constant correction process going on to keep the two signals C and J in phase. It takes the Phase Lock Loop up to 50 us to lock on to the Read Clock/Data for a "1111 or 0000" pattern and up to 100 us for a "1010" pattern. The loop operates basically the same for either MFM or DF operation, the only differences being that the data cell time for MFM is 2 us (as opposed to 4 us for DF), so one-shot 3L produces a 500 ns wide pulse (C) for MFM and a 1 us wide pulse for DF, and J differs correspondingly. For MFM the VCO output G is divided by two and for DF G is divided by four. Figure 7-4 shows the locations of TP1 and TP2 so that the Data/Clock pulse and the VCO CLK pulse can be compared for maintenance purposes.

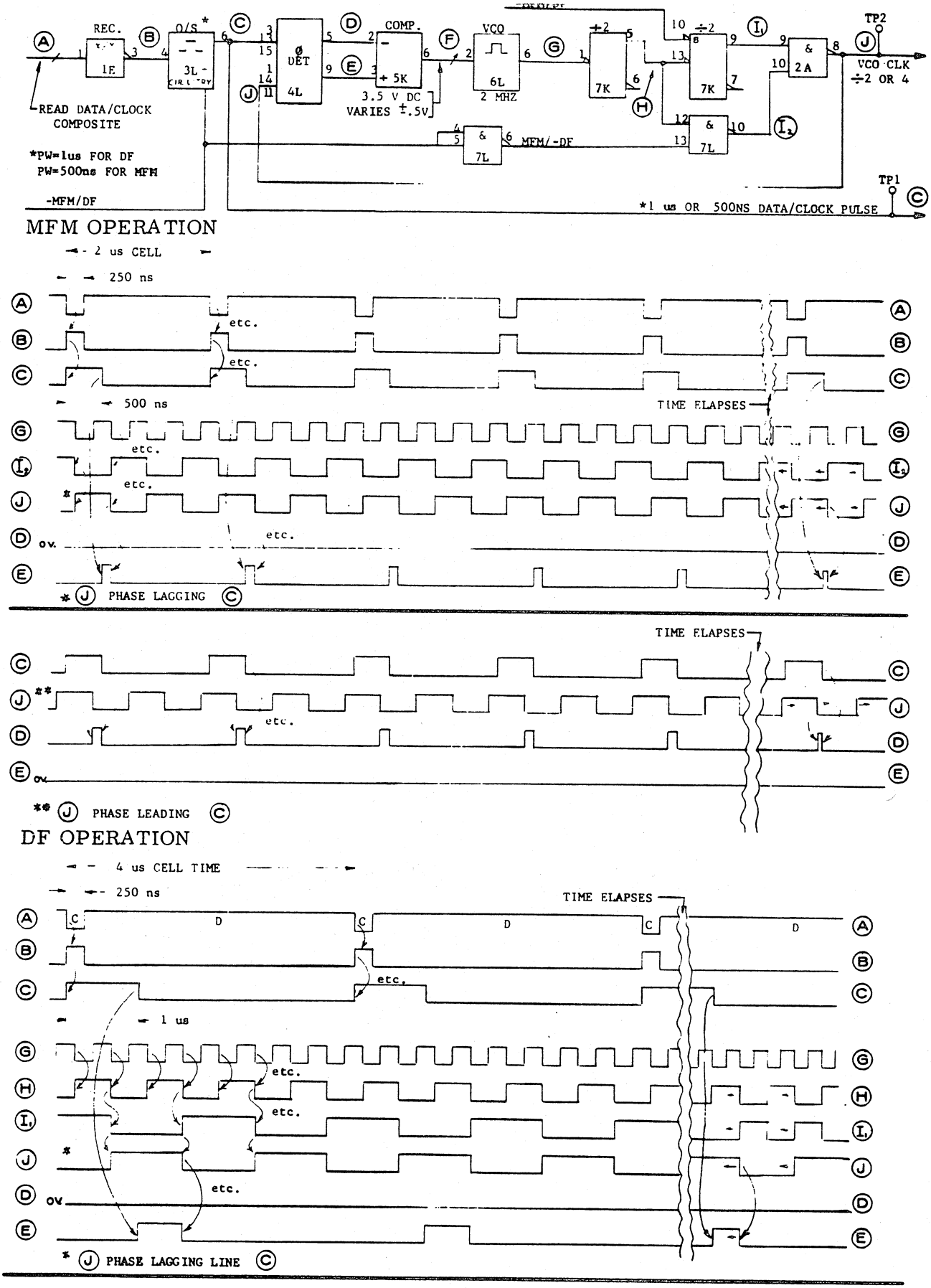


Figure 4-12. Phase Lock Loop Block Diagram and Timing

4.6.2 READ CLOCK/DATA SEPARATION

The second step in the data recovery process is the separation of the clock from the data in the information being read from the Diskette. Figure 4-14 is the circuit which generates the NRZ Data Signal and NRZ CLK (becomes REG CLK) which are shown in the timing diagram referred to in this section. The Diskette is formatted at the beginning of every sector with a special pattern of clock and data called a preamble which the Adapter logic uses to establish the proper timing relationship between the NRZ clock (VCO CLK ÷ 2 or ÷ 4 inverted) and data time in the READ Clock/Data signal. The preamble pattern is a special combination of clock and data pulses. In a DF recording the preamble is 6 "zero" data bytes and in MFM recording the preamble is 12 bytes of "55". Both of the two preambles would look the same when looked at on an oscilloscope, that is, a string of equally spaced pulses. In DF the pulses would be clock pulses, but in MFM the pulses would be data "ones". The frequency of the pulses would be the same for DF and MFM. The preamble follows immediately after the "FF" bytes used by the Phase Lock Loop circuits to phase sync the VCO clock to the READ Clock/Data signal as described in paragraph 4.6.1.

Figure 4-13 shows the timing of the early stages of data recovery where the READ Clock/Data signal is clocked serially into a deserializing register (see sheet 13 of Figure 5-4) using a clock that is twice the normal frequency used when normal data is being recovered from the disk. Therefore something is clocked into the register at both clock time and data time. Figure 4-13 shows an MFM data pattern of one "F" and a "55" byte. When the pattern of clocks and data bits is decoded as 10001000 (D7 .... D0) for MFM and 01010101 for DF, a signal -SYNC is generated which serves to get the .5 mHz MFM CLK and the .25 mHz DF CLK in bit sync with the NRZ DATA. Once bit sync is achieved and the Address Mark has been detected VFO CLK will not be used as REG CLK, but .5 mHz CLK for MFM and .25 mHz for DF will be used instead, as these are the correct frequency to clock only at data time and not at clock time. The selection is made by gates 6G and 7G on sheet 10 of Figure 5-4 schematic. For DF operation the basic ideas of Figure 4-13 are the same. The data pattern of line C would be slightly different and the pattern in the shift register at time T would be 01010101 as mentioned above. Everything else would operate the same. On sheet 13 of Figure 5-4, decoder 5H decodes the MFM pattern and 6J decodes the DF pattern.

4.6.3 DETECTING THE ADDRESS MARK

Once bit sync has been achieved a counter (9B on sheet 9 of Figure 5-4) counts 32 bits of preamble (data for MFM; clocks and data for DF). When 32 bits have been counted the search for the Address Mark begins. The READ Clock/Data signal continues to be clocked twice each data cell into the SERDES register 3H in order that a particular pattern of clock and data bits may be detected as the Address Mark. The pattern searched for has missing clock bits which would never legally be missing in normal data, even in MFM which has missing clocks as part of its regular data format. The "illegally" missing clocks plus regular clocks and data form the pattern 01000100 (D7....D0) for MFM and 11101010 (D7....D0) for DF. These patterns are decoded by 7J and 7H respectively on sheet 13 Figure 5-4, creating the signal AM1 when the correct pattern is detected. See timing diagrams of Figure 4-15. AM1 creates EN SYNC 1 FF CLK which disables the search for the AM1 pattern. See sheets 9 and 12 of Figure 4-5. EN SYNC 1 flip-flop (7E) is reset by EN SYNC 1 FF CLK and the next 1 MHz clock after AM1 goes high.

The second half of the Address Mark is called AM2 and is a code which indicates whether the data to follow is sector address, sector data or a deleted record. The Address Mark being considered here is the one preceding the sector address. AM2 in this case is detected when the logic decodes 11111101 for DF and 10100010 for MFM. This decoding is done by 6H and 5J respectively on sheet 13 of Figure 5-4. When AM2 goes true it sets flip-flop 7E (Figure 5-4, sheet 11) whose output CRC ON/AM READ goes to PPI #3 to inform the microprocessor that the Address Mark preceding the sector address has been read. REG CLK at this point changes from the 1 mHz or .5 mHz NRZ clock to either the .5 mHz clock for MFM or the .25 mHz clock for DF. See gates 6G and 7G on sheet 10 of Figure 5-4. NRZ DATA is now clocked into the SERDES register during data time only - no clock pulses (or lack of pulses) are clocked into the SERDES register now. The data clocked into the SERDES register now is the sector ID which is transferred to the Microprocessor through PPI #1 (sheet 8, Figure 5-5) in parallel eight bits at a time. Counter 8D (sheet 10, Figure 5-4) counts each eight bits and indicates byte frame time. At the same time the data is clocked serially into an eight-bit delay register 9H (sheet 12, Figure 5-4) from where it goes to the CRC Generator/Checker (sheet 11, Figure 5-4). CRC ON/AM READ enables the CRC Generator/Checker and it checks the ID and compares with the two CRC bytes appended to the ID field.

After the ID field comes a gap of FF bytes and field of "0" bytes used to bit sync the clock again (see format, Section 4.2.9.5). After the "0" bytes is an Address Mark, the first part of which is identical to the Address Mark preceding the ID field. The "0" bytes appear as "55" bytes in MFM, but in actuality the pulse/no pulse pattern is the same. Bit sync and the search for AM1 are accomplished as described previously. AM2, however, is not decoded by the hardware as it was for the ID field Address Mark, but is decoded by the firmware. Once it has been determined that AM2 has been found the change of clock frequency is accomplished as before and the data field is read into the microprocessor memory. If the correct sector address was not found the search is continued for the correct sector.

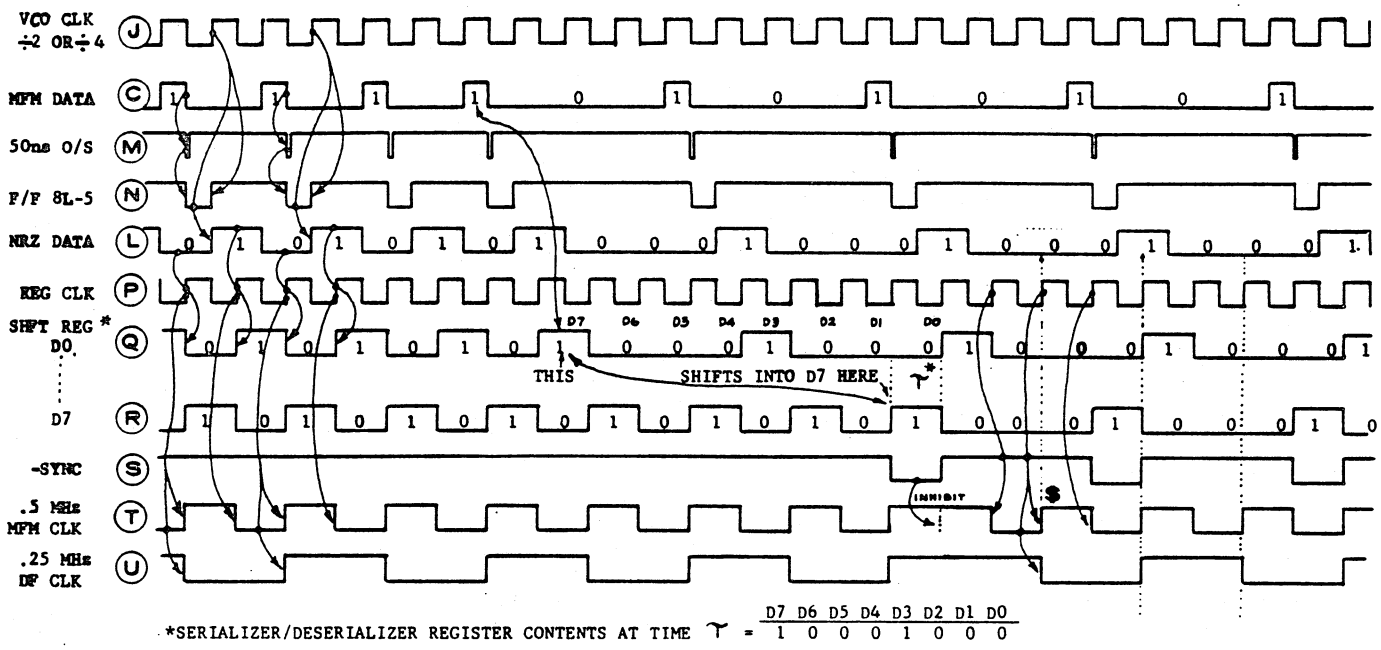
4.6.4 READ DATA HANDLING

The remaining read process consists of serially loading the data shift register, 3H (sheet 13, Figure 5-4) and transferring the 8 bits in parallel to PPI #1 and then to the microprocessor memory using a DMA cycle. The UP-DOWN COUNTER (5G and 5F, Figure 5-5, sheet 9) is preset until the Address Mark is read to a count of 11111110, the zero being the least significant bit.

The count sequence is:

Preset	254
1st	255 ← 1st carry
2nd	000
	001
	002
	003
	:
	255

A DMA cycle increments the counter. A Host transfer decrements the counter. Host can transfer data when count is above zero. If the count decrements from 0 to 255, a borrow is generated, stopping host data transfers until the next carry (counter increments from 255 to 0). FF 4G counts 2 carrys without a borrow in between and indicates a transfer timing error if it occurs (Sheet 10, Figure 5-5).



TIMING SEQUENCE:

1. MFM data from disk triggers 50 ns one-shot M.
2. Falling edge of M triggers first 8L flip-flop; pin 5 goes low. See simplified logic of Figure 4-14.
3. VCO CLK ÷ 2 or ÷ 4 (÷ 2 for MFM) retriggers 8L flip-flop and pin 5 goes back high.
4. While 8L-5* is low 8L-6 is high so the second 8L flip-flop is reset causing 8L-7 to go high. NRZ DATA is the 8L-7 signal and is high when a "1" is detected in the MFM data signal C. NRZ DATA remains low as long as MFM data is "0".
5. REG CLK, which is NRZ CLK after passing through some gating, clocks the NRZ DATA state into the Serializer/Deserializer Shift Register. D0 being the first flip-flop (Q in the timing), and D7 the last (R).
6. The contents of the SERDES register is continually decoded. When the pattern of clocks and data zeros equals 10001000 (D7 through D0), the -SYNC signal occurs (S). See sheet 9 of Figure 5-4, decoder 5H.
7. "-SYNC" is used to get the .5 mHz and .25 mHz clocks in proper phase with the NRZ DATA signal. Flip-flop 7C (T, U above) on sheet 12 of Figure 5-4 is prevented from counting RD/WRT CLK (same as REG CLK) until the proper time so that the proper phase relationship with NRZ DATA exists. This occurs at the point "$" on line T.

*Refer also to Figure 8-14.

Figure 4-13. Data/Clock Separation Timing During Preamble of Data Sector

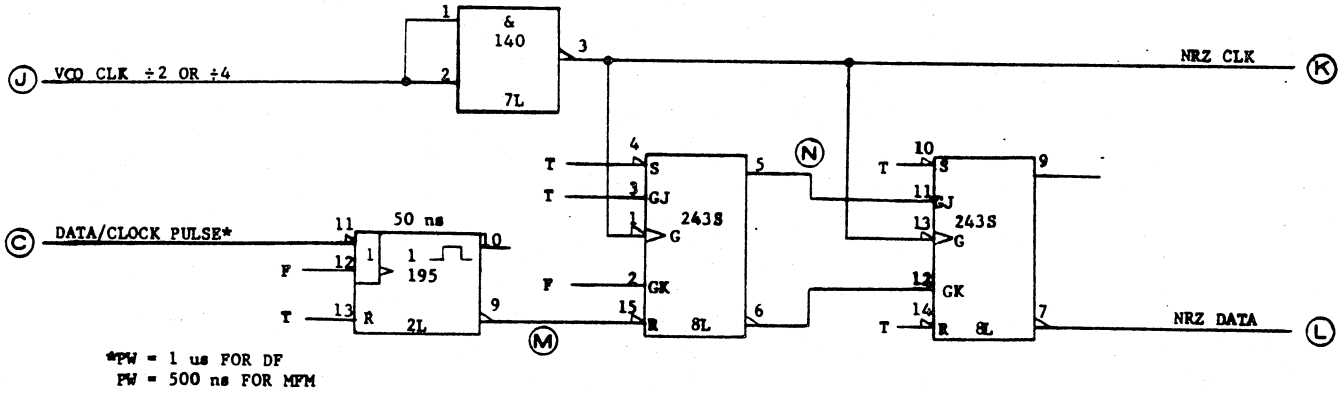
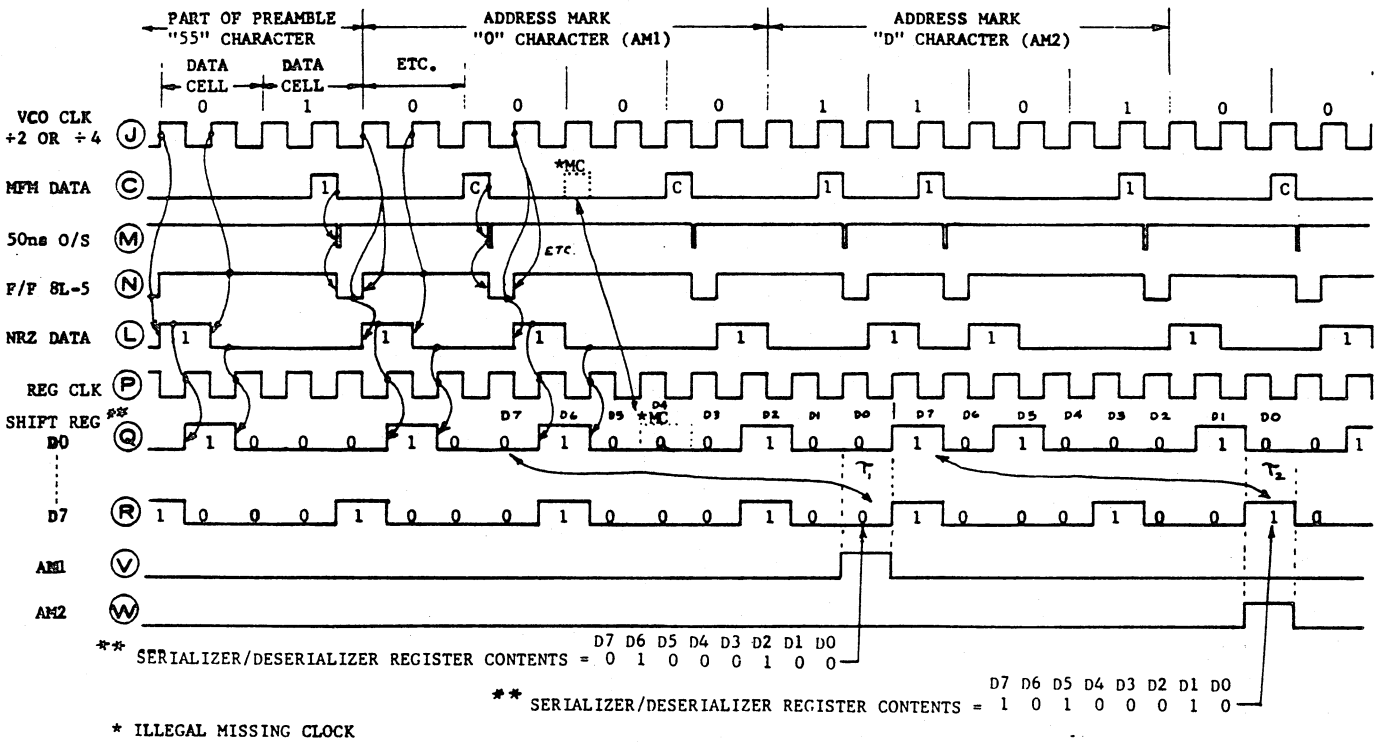


Figure 4-14. Clock and Data Separation Circuit



TIMING SEQUENCE:

1. See Figure 4-13. Items 1 through 5 apply exactly the same here.
2. The contents of the Serializer/Deserializer Register are continually decoded through the preamble until time T_1 when the eight bits in the register are 01000100 (D7 through D0). In normal data this pattern could not legally occur. It can only occur when clocking twice each data cell time as is done while searching for the Address Mark.
3. Address Mark AM1 is detected at time T_1.
4. The data is continually shifted through the SERDES Register until T_2. Then pattern 10100010 is decoded which is AM2. If the data were clocked into the SERDES Register only once each data cell time the two hexidecimal characters 0D would be in the register.
5. After AM2 (timing not shown) the REG CLK would be .5 mHz, which is half the frequency shown in this diagram. The sector ID would be then clocked through the register.

NOTE

For DF operation the byte decoded at T_1 time would be 11101010 (the three zeros are missing clock pulses) and at T_2 time would be 11111101.

Figure 4-15. Timing for Detection of Address Marks AM1 and AM2 Preceding the Sector Address Field (MFM Operation)

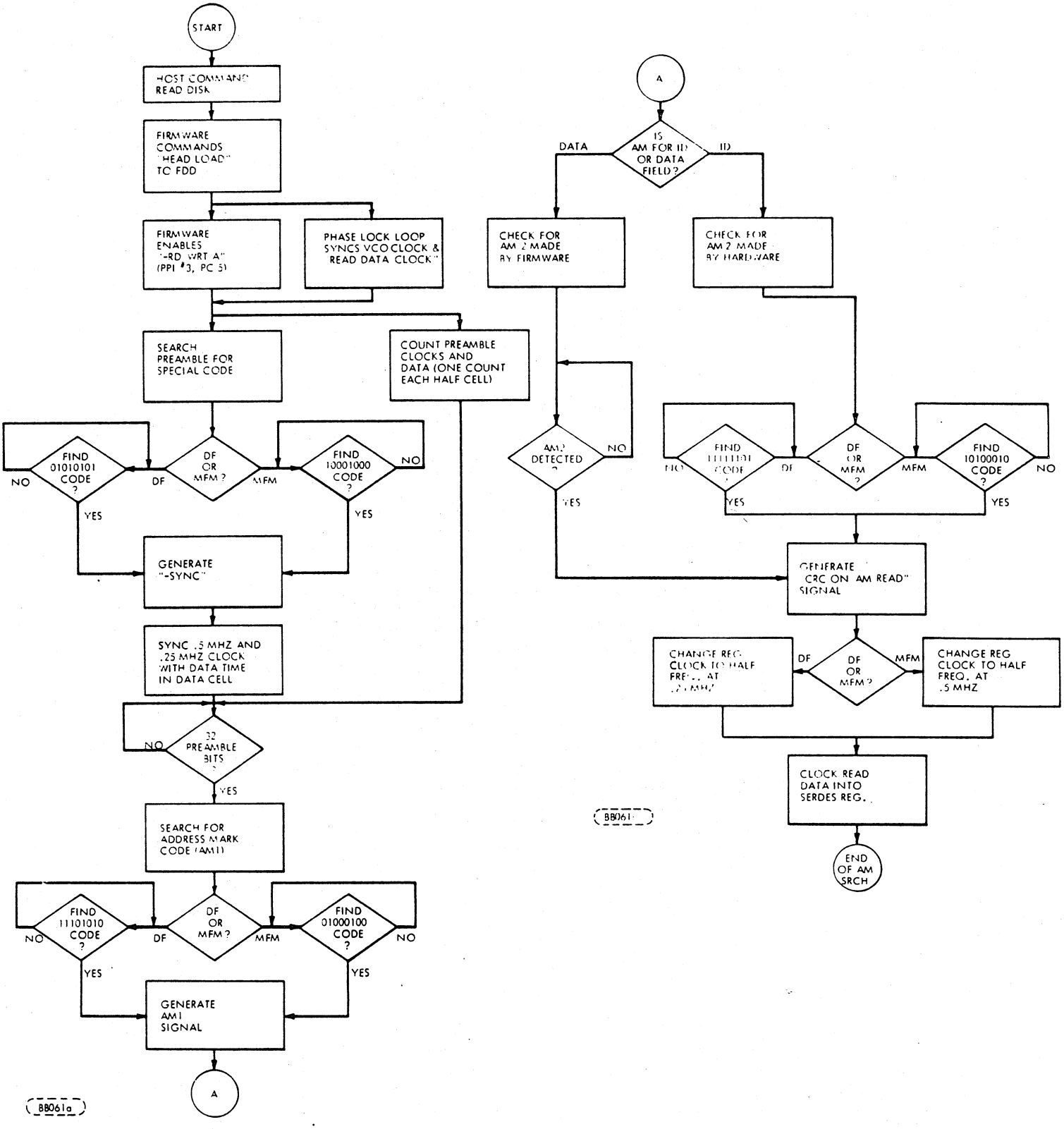


Figure 4-16. Address Mark Detection Flow Chart

4.7 WRITE FUNCTION CONTROL

Much of the write control circuitry utilizes some of the data recovery circuitry already discussed and some of the timing comes from circuits generating timing for data recovery circuits. Refer to the schematic diagrams, Figures 5-4 and 5-5, as well as timing diagrams in this section and the Appendix for aid in understanding the operation of the write circuits. Section 4.10 gives more explanation on the operation of the 8080 Microprocessor and DMA circuits and should also be referred to. A general description is given in Section 4.2.9.7, "Write Disk".

4.7.1 PRELIMINARY OPERATIONS

The start of the Write Data Function is the transfer of data from the Host into the FDA memory buffer. This is covered in sections 4.3 and 4.10. Head positioning is covered in section 4.8 and will not be discussed here. This description will commence with setting the write current.

4.7.1.1 Set Drive Current

If the write head is positioned to a track number 43 or greater low write current must be used. Firmware makes this decision and enables PC4 of PPI #3. PC4 after gating becomes LOW CURRENT which is active in the selected unit. LOW CURRENT also enables the write compensation logic.

4.7.1.2 Input SERDES Status

The status of the data recovery operation is sent to the microprocessor via PPI #3 port B (see Table 4.2). Firmware is waiting for indication that the AM search is complete.

4.7.1.3 Initiate Address Mark Search

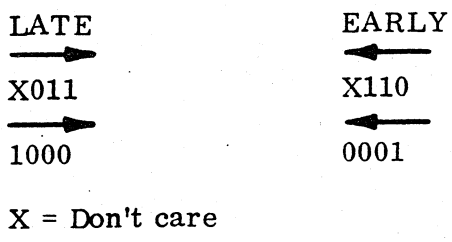
Before actual writing of data can begin the proper sector must be found. This requires the same Address Mark search as performed for a read data operation. Firmware turns on -RD/WRT A to start the AM hunt. When one of the AMs is found the hardware logic must check it to see if it is the AM for the sector ID field. If the wrong AM has been found the search for the preamble is initiated and then a new search for the correct AM. ID READ stays true until the correct address is found and it is read into the memory and checked. If the correct address is not found by the end of one revolution of the disk it is an error and the AM search ceases. When the correct AM and ID is found, stored in memory and checked for correctness and CRC agreement, firmware turns off -RD/WRT A and ID READ. Disk DMA DONE from the DMA control Figure 5-5, sheet 10, initiates a firmware delay loop while the space before the zero bytes goes by the head. Writing data will begin with the zero bytes preceding the data field AM. While the delay loop is on, the first zero byte is loaded into port A of PPI #2. Refer to Appendix A for timing on the write sequence.

4.7.1.4 Turn On DMA "ID READ"

Firmware enables PC6 of PPI #2 which is the ID READ signal. This enables the clock input of the DMA request flip-flop (6E, Figure 5-5, sheet 11). When AM2 occurs it sets flip-flop 7E which switches the source of the REG CLK signal so only data is clocked into the SERDES register rather than clocks and data as was the case during AM search. ID READ enables AM2 to set 7E. The ID information is transferred to the microprocessor through PPI #1 under control of the DMA request control circuitry Figure 5-5, sheet 11. Refer to Section 4.6.2 which also describes reading the ID.

4.7.2 WRITE SEQUENCE

When the decision is made by firmware that the sector address is the correct one sequences are entered which control the actual writing. The preamble of six "0" bytes and the data field address mark must be written, and then the actual data. The microprocessor operating through the LSI SYSTEM CONT/BUS DRIVER module (both on M.P. #2) initiates the accessing of memory for a write and the timing of the write operation by programming the 8257 DMA controller, then activating it at the proper time with "-EN RD/WRT". The DMA then takes over all of the control of the Write operation. Figure 4-18 shows the blocks of circuitry involved in the write operation. Data bytes and control bytes are stored in the PPI modules where they reside until being activated at the proper time by the DMA controller signals. See Section 4.10.2 for more details on the DMA System. When signaled to do so the control signal REG S/L loads the data from PPI #2 into the serializer/de-serializer register in parallel and shifts the data out again in series. The data is also shifted in series through the CRC Generator where CRC bytes are generated for inclusion at the end of the data field. During the preamble nothing is shifted through the SERDES Register or the CRC Generator. Only clock bits are sent on the WRT NRZ DATA line since the data is all zeros. See gate 8F Figure 5-4, sheet 11. REG S/L is generated by an 8 counter that counts bit times (8D, Figure 5-4, sheet 10) to provide byte frame reference logic which transfers each byte of data in parallel into the SERDES Register 3H. On other than the eighth bit count from 8D, REG S/L shifts the data in the SERDES Register, either in or out, whichever is applicable. Also during the eighth count time a DMA request is generated so that the next byte of data can be loaded into PPI #2 while the present byte is shifted out of the SERDES Register. WRT NRZ DATA serially transfers data from the CRC Generator to a seven flip-flop shift register which divides the NRZ write data into half cells. That is, if the first flip-flop, 6B-9, contains a data bit, the next flip-flop contains a clock and the next data, and so on. During the transmission of the Address Mark to the FDD there must not be any write compensation, so that data is made to bypass the compensation circuits by control of the EN AM WRT signal out of PPI #2, PC7. In DF operation the clock/data patterns which would require write compensation never occur so DF write data passes through without compensation. The NRZ to MFM conversion and write compensation circuits are found on sheets 14 and 15 of Figure 5-4. On sheet 14 MFM encoded data is gated out of 4D-8 as the PATT signal which is retimed by flip-flop 5A-5 (sheet 15) with the pulse width being set to 50 ns. The data from 5A-5 is either gated out directly as the early data or goes through a delay line (3A on sheet 15) to produce the on time or late data. Write compensation is required to reduce the effect of peak shift out of the head due to the reduced window of MFM data. The window is defined as the total amount of time that is allowed for the bit to appear and be recognized. The window of MFM is 1 us as opposed to the double frequency window of 2 us. The amount of compensation best suited to the present heads and media is 250 ns. This compensation is applied to data patterns that otherwise would result in a large peak shift of the data pulses. The circuit on sheet 14 of Figure 5-4 "looks" at three bits on each side of a reference bit (in F/F 6D-5) and determines whether to shift or not. The following patterns are compensated (bit shifted) in the direction of the arrow.



X = Don't care

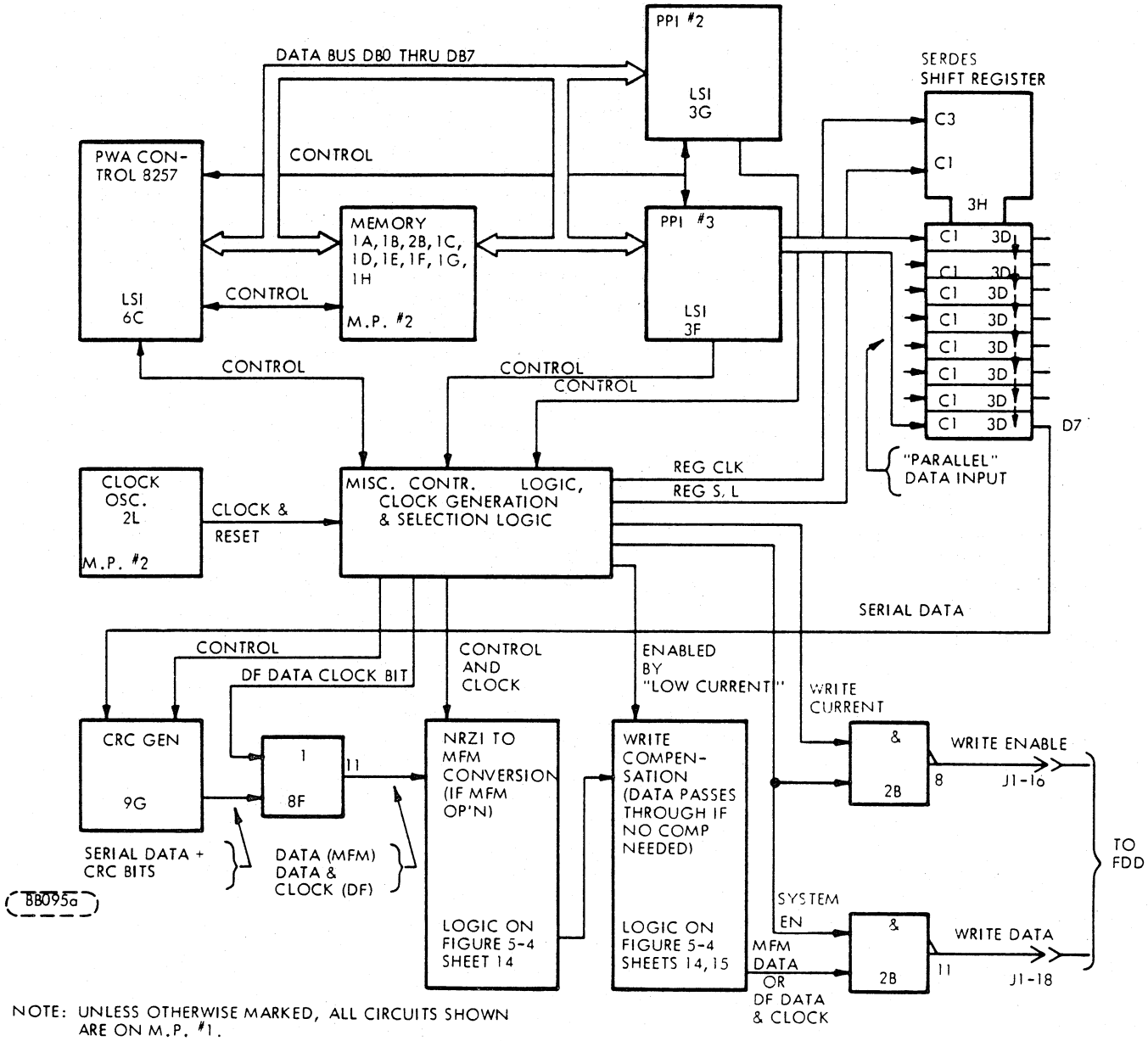
When a flux transition pattern of "110" is written on the disk the second "1" is pulled toward the "0". Write compensation shifts this "1" in the opposite direction the amount of the expected shift. The half cell data/clock information in the aforementioned seven flip-flops is decoded by the gates of 5B, 5C, 5D and 4D to form logic control signals that gate the data out to the FDD either before the delay line (early), 250 ns into the delay line (on time) or 500 ns later at the end of the delay line (late).

LOW CURRENT controls whether compensated or uncompensated data is written. Writing on tracks 42 to 76 requires compensation and writing on tracks 00 to 41 does not.

4.8 HEAD POSITIONING

Head positioning control is provided by the 8080 microprocessor. Track Address information is transferred from Host to FDA as described in Section 4.2.2 and 4.2.9. Figure 4-2 shows timing for positioning the heads following a MASTER CLEAR. Figure 5-4, sheets 6 and 7, shows the logic diagram containing head positioning logic.

Head positioning commands come from PPI #3, PC2 and PC3. PC2 and PC3 are enabled by microprocessor firmware. Based on information received from the Host, one of the FDD units is selected. The microprocessor sends the proper bit to PPI #3 to accomplish the selection. FDD 1 is selected by PA0, and FDD 2 is selected by PA1, FDD 3 is selected by PA2 and FDD 4 is selected by PA3. The STEP and DIRECTION signals are logically selected by the microprocessor which sends the proper bit pattern to PPI #3 to generate the STEP and DIRECTION signals. PC1 of PPI #3 provides the HEAD LOAD signal to the selected FDD.



NOTE: UNLESS OTHERWISE MARKED, ALL CIRCUITS SHOWN ARE ON M.P. #1.

Figure 4-17. Circuit Blocks Used in Write Sequence

4.9 INDEX PULSE PROCESSING

Index pulses from the selected FDD unit come to the microprocessor through PB1 of PPI #2. Refer to the schematic diagrams of Figure 5-4, sheet 2. The microprocessor makes an accurate check on the speed of the FDD spindles by checking the time between index pulses with firmware programming. Index pulses should occur every 166 milliseconds and this time interval is checked within ±4% by the 8080 firmware. If the speed is not correct this fact is conveyed to the Host by dropping status line READY, indicating a not ready condition exists (see Section 3.11). When the door of one of the units is opened the spindle for that unit stops, sending UNIT READY INTERRUPT to M.P. 1. This interrupt signal sets one of the latches of 1G (Figure 5-4, sheet 4), and the status of the latch of the selected unit is sent to the 8080 microprocessor through PPI #2. This tells the 8080 that the diskette may have been changed and the Host is informed so that it can alter its procedure accordingly. The set state of a not ready latch (1G) is not reset until after the status of a not ready unit is sent to the Host informing it of the not ready history of the unit.

The index pulse is also used to time index to index write operations. The circuitry for this is on sheet 8 of Figure 5-4. Flip-flops in IC 4G are clocked with the index pulse. Flip-flop 4G-6 is set by the first index pulse after -IND TO IND enables both flip-flops, and 4G-10 is set by the second index pulse after being enabled. Flip-flop 4G-6 is reset at the same time 4G-10 is set. Flip-flop 4G-10 stays set until firmware inactivates -IND TO IND at PPI #3. Flip-flop 4G-10 is the index to index done signal (IDX TO IDX DONE) which informs the firmware through PB4 of PPI #3 that an index to index time period has elapsed.

4.10 MICROPROCESSOR SYSTEM OPERATION

This section gives more details on the Microprocessor system and DMA system and how they operate together. See also vendor 8080A system user manuals. The 8080A Microprocessor (M.P. 2, location 1K) controls the operation of the FDDS unit. Instructions executed by the 8080A in operation of the FDDS together with any permanent data required by the program are stored in ROM units. The program instruction set stored in ROM is referred to in this manual as the "Firmware", as those instructions cannot be changed in the process of executing the 8080A program. Any temporary instructions and transient data generated during the execution of the 8080 program are stored in RAM units. The RAM units are also used as buffer storage for data transferred to/from Host and FDD units. A number of other chips besides the 8080A are required to complete the Microprocessor system and these are discussed briefly in the following subsections.

4.10.1 MICROPROCESSOR SYSTEM

The microprocessor system includes the peripheral packages required to complete the 8080A working system. The microprocessor system packages include the following:

- Clock Generator - The 8224 produces the two phase 8080A clocks, reset signals and 18 MHz system clock.

- Memory - The memory system has 512 bytes of RAM (8111A-1) and 3K bytes of ROM. There are two spare ROM locations, IE, ID. Addressing of memory and the peripheral devices is achieved as shown in Table 4-5. The main address decode hardware is 3J (7442) and 3K (7442).

Table 4-5. Memory Mapped I/O

CHIP SELECTED	ADDRESS BIT F E D C B A 9 8 7 6 5 4 3 2 1 0
ROM 1H	0 0 0 0 0 0 . .
ROM 1G	0 0 0 0 0 1 . .
ROM 1F	0 0 0 0 1 0 . .
ROM 1E	0 0 0 0 1 1 . .
ROM 1D	0 0 0 1 0 0 . .
PPI 8C	0 0 1 Z Z . . .
PPI 3G	0 1 0 Z Z . . .
PPI 3F	0 1 1 Z Z . . .
DMA 6C	1 0 0 . . . . .
PORT 1 4K	1 0 1 . . . . .
RAM 1A, 1B	* . . . 1 0
RAM 2B, 1C	* . . . 1 1

*RAM may also be selected any time address bits F, E and D are not all zeros.

Z - Selects the port within the PPI in accordance with the following table:

	ADDR BIT C	B
Control	0	0
Port C	0	1
Port B	1	0
Port A	1	1

- System Controller - The 8228 (M.P. 2, 1J) is the system controller for the 8080A providing timing signals for the various 8080A operations utilizing the data bus and memory address lines.

- Interrupt Instruction Port - The 8212 (2C) is acting as an interrupt instruction port. The 8080A system, upon recognizing a pending interrupt, will input via the data bus a Restart instruction. This instruction basically is encoded with the interrupt routine starting addresses. The restart address is eight times the value of the three bit address. These three bits are encoded as a function of the TAG leads with two overriding hardware leads. The highest priority is the DMA INT which will override the other three. The second highest priority is the IDX/XFER ERROR which overrides the three TAG lead interrupts. Note that when the TAG lines are coded for data (both lines LOW) no interrupt is generated for the 8080A since Host data transfers are handled by the DMA chip (8257). See Table 4-6.

- Direct Memory Access Controller - The 8257 controls access to memory by devices other than the 8080A. The 8080A accesses memory through the 8228. The 8257 is programmed by the 8080A and activated through the 8228 and PPI #3 (3F). The DMA system is described in more detail in section 4.10.2.

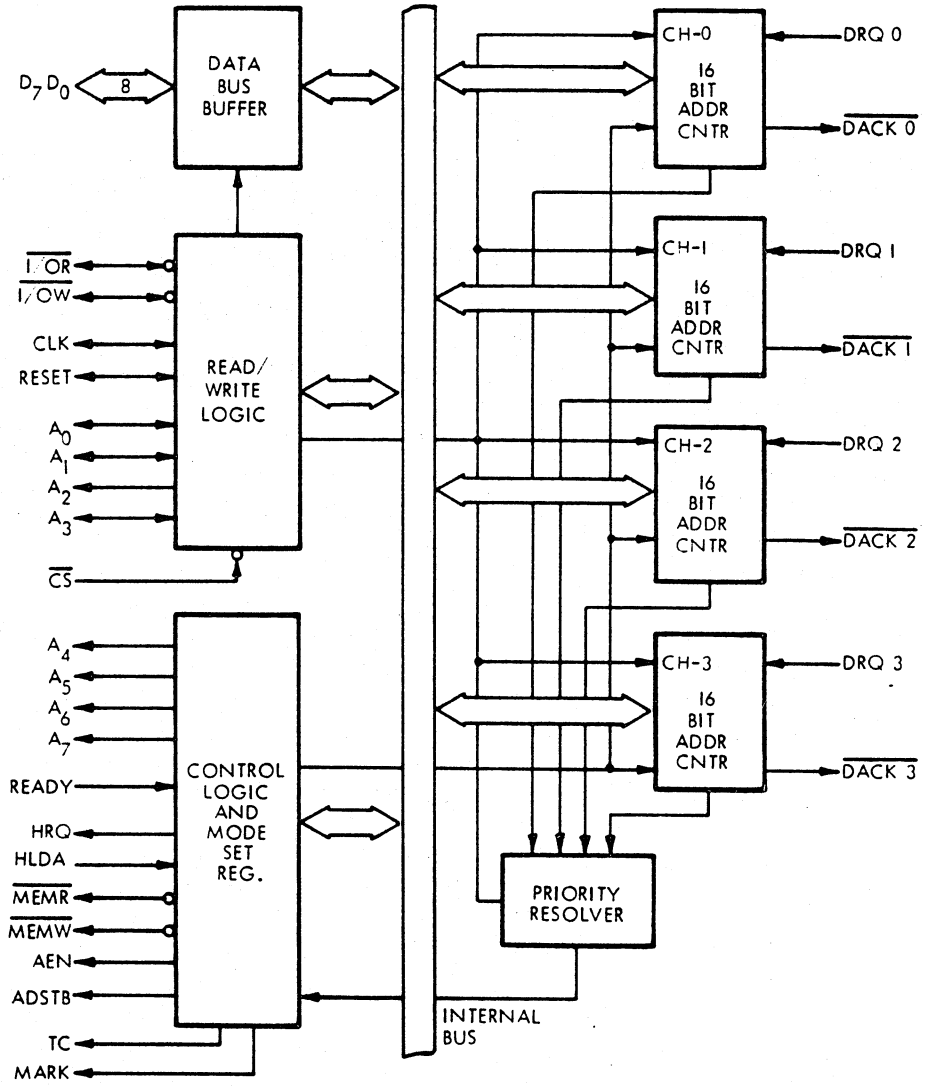
Table 4-6. Interrupt Instruction Port Inputs/Outputs

+TAG 1 3D-9*	+TAG 2 3D-4*	-DMA INT 3D-2*	-IDX/XFER ERROR 3D-5*	2C-9*	2C-16*	2C-18*	INTERRUPT TYPE
H	H	L	L	L	H	H	DMA
H	H	L	H	L	H	H	DMA
H	H	H	L	H	L	L	IDX/XFER ERROR
H	H	H	H	H	H	H	FUNCTION
H	L	L	L	L	H	H	DMA
H	L	L	H	L	H	H	DMA
H	L	H	L	H	L	L	IDX/XFER ERROR
H	L	H	H	H	H	L	TRACK
L	H	L	L	L	H	H	DMA
L	H	L	H	L	H	H	DMA
L	H	H	L	H	L	L	IDX/XFER ERROR
L	H	H	H	H	L	H	SECTOR

*Figure 5-5, sheet 6.

4.10.2 DMA SYSTEM

The Direct Memory Access (DMA) System enables the hardware to access the memory without using the 8080A. This is done by requesting a hold from the 8080A which causes the address and data buses to be freed. The 8080A responds with a hold acknowledge back to the DMA system. A DMA cycle is required to enter all data from devices and Host into memory. Also in the case of a write, the data to be written is loaded into a PPI from memory with a DMA cycle.



D7-D0	DATA BUS
A7-A0	ADDRESS BUS
IOR	I/O READ
IOW	I/O WRITE
MEMR	MEMORY READ
MEMW	MEMORY WRITE
CLK	CLOCK INPUT
RESET	RESET INPUT
READY	READY
HRQ	HOLD REQUEST (TO 8080A)
HLDA	HOLD ACK. (FROM 8080A)

AEN	ADDRESS ENABLE
ADSTB	ADDRESS STROBE
TC	TERMINAL COUNT
MARK	MODULO 128 MARK
DRQ_3-DRQ_0	DMA REQUEST INPUT
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA ACKNOWLEDGE OUT
$\overline{CS}$	CHIP SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BBI58

Figure 4-18. 8257 DMA Controller Block Diagram

The DMA System is under the control of the 8257 Programmable DMA Controller on M.P. 2, location 6C. The 8257 has 4 DMA channels with control assignments as follows:

Channel 0 - Host Data
Channel 1 - Status Requests
Channel 2 - Disk Data
Channel 3 - Autoload ch. 2 for next disk operation

Each channel contains a 16 bit memory address register and a 16 bit terminal count register. The 8080 initializes the registers and then stores in them the starting memory address and the number of bytes to be transferred during the pending memory access. The value loaded into the low-order 14-bits of the terminal count register specifies the number of DMA cycles minus one before the Terminal Count (TC) is activated. For example, a terminal count of 0 would cause the TC output to be active during the first DMA cycle for that channel. The most significant two bits of the terminal count register specify the type of DMA operation for that channel:

BIT 15	BIT 14	TYPE OF DMA OPERATION
0	0	Verify DMA Cycle
0	1	Write DMA Cycle
1	0	Read DMA Cycle
1	1	(Illegal).

For data transfers to/from Host, TC (pin 36, 6C) sets the HOST DMA DONE flip-flop and for data transfer to/from FDD, TC sets the DMA INT/EN CRC flip-flop. The first flip-flop informs the 8080A that the DMA is done through the PPI #3. The second flip-flop interrupts the 8080A and sets up a RESTART instruction in the 8212 when the 8080A comes back with an interrupt acknowledge through the 8228 system controller. Though TC indicates that the memory access is complete for data transfers to and from the disk, CRC bytes must be stored in memory or sent to the disk, so disk DMA DONE is not sent to PPI #3 until the CRC bytes are stored in memory or sent to the disk.

The 8257 DMA Controller does not have enough memory address capacity to address the total memory of the FDDS so an 8212 chip (4C) is used as an address port for the 8 high order address bits. The 8257 has its own address port for the lower order address lines.

Once the 8080A has programmed the 8257 with the starting memory address and the number of bytes to be transferred the typical sequence of events is as follows:

1. DISK DMA REQ or HOST DMA REQ comes into the DMA.

2. DMA HOLD REQ sets HOLD REQ flip-flop. HOLD REQ goes to 8080A.

3. The 8080A sends back HOLD ACK and lets the data and address buses float.

4. The 8257 stores the high order address bits in the 8212 (4C) and puts the low order address bits on its own address lines.

5. A device is selected in accordance with Table 4-5. For example, if the DMA is controlling the loading of PPI #2, the address lines would simultaneously select an address in RAM, PPI #2 and Port A of PPI #2.

6. Data is put on the bus, by memory if an output, by PPI if an input to memory.

7. The 8257 activates -MEM R or -MEM W to the memory and -I/O RD or -I/O WRT to the PPI. This indicates that the data is stable on the lines. -MEM W and -I/O RD causes data to be transferred from PPI to RAM, for example.

8. Data is transferred from PPI #2 to the SERDES Register (for write) or from SERDES Register to PPI #2 (for read) under control of a signal (REG S/L) from the eight bit counter 8D (M.P. 1). Counter 8D counts bit times and during the eighth count the parallel data transfer takes place to/from the SERDES from/to PPI #2. A DMA request is also made at this same time so that the next byte can be transferred from memory to PPI #2 during the time data is being shifted out of the SERDES.

V
DIAGRAMS

5.1 INTRODUCTION

This section contains the Interconnection Diagram, a table of commonly used Integrated Circuits, a key to the logic diagram symbology and Printed Circuit Board documentation.

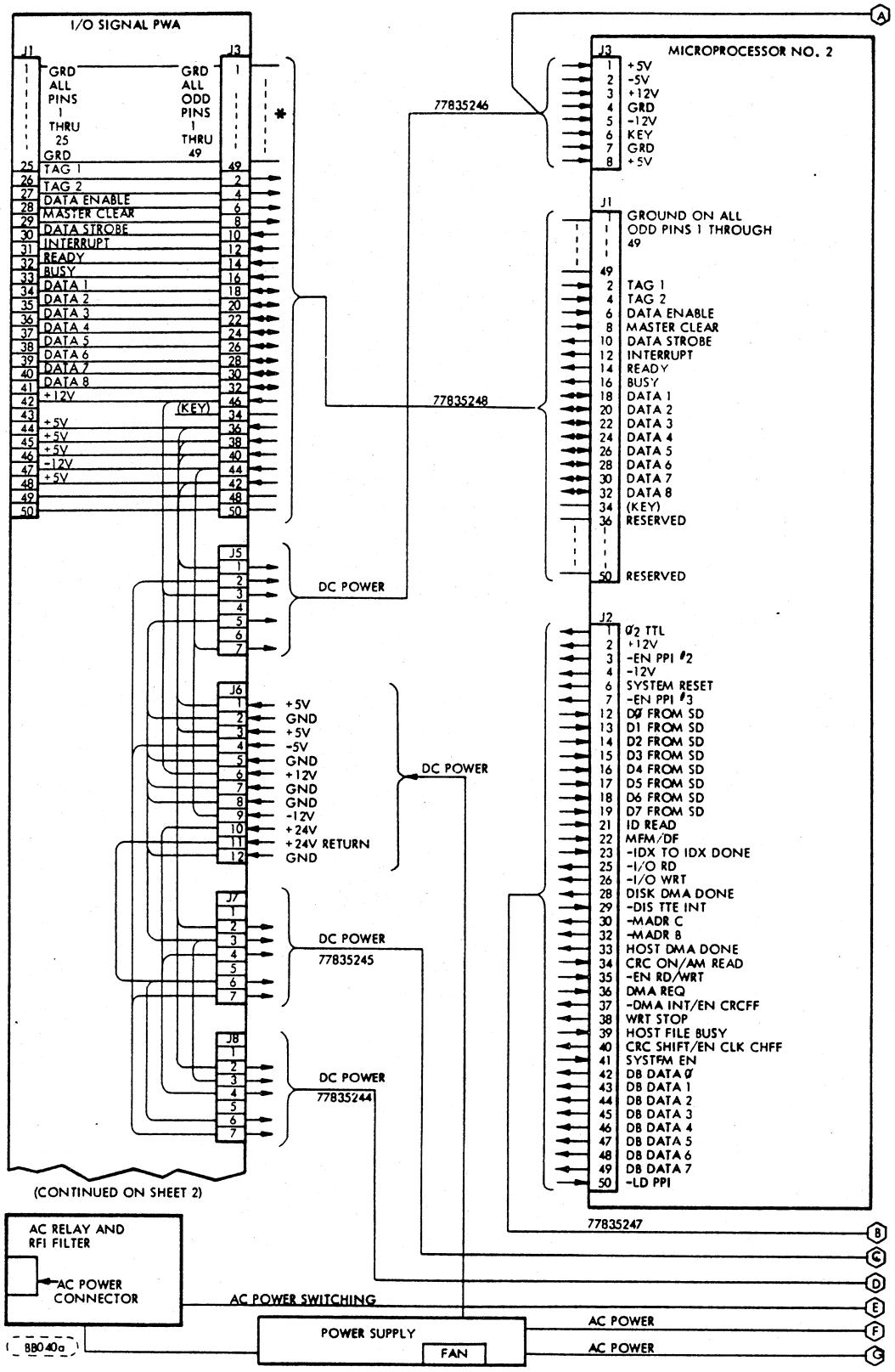
5.2 INTERCONNECTION DIAGRAM

Refer to Figures 5-1 and 5-2 for signal interconnection diagrams.

5.3 CIRCUIT BOARD DOCUMENTATION LIST

Documentation for the printed wiring circuit boards listed below is included in Section 5.5.

CIRCUIT BOARD TITLE	FIGURE LOC.	ASM NO.
PWA Micro Processor No. 1	5-4	75896500-8
PWA Micro Processor No. 2	5-5	758966 02-2
I/O Printed Wiring Asm. (No. 1)	5-6	77834600-7
I/O Printed Wiring Asm. (No. 3)	5-6a	75895750-0
Schematic, FDDS AC Pwr Inter.	5-8	
Power Supply PWA Type 6 VZN	5-9	76845400-1
Power Supply PWA Type 6 VYN	5-10	76845000-9
Interconnect Schematic for P/N 76835500 Pwr Sply	5-11	
I/O PWA Asm. (No. 2, Slave)	5-7	77834450-7
I/O PWA Asm. (No. 4, Slave)	5-7a	75895800-3



* ALL J3 GROUNDS TIED TO FRAME GROUND ON I/O PWA NO. 3 ONLY.

Figure 5-1. Interconnection Diagram (Master) - (Sheet 1 of 2)

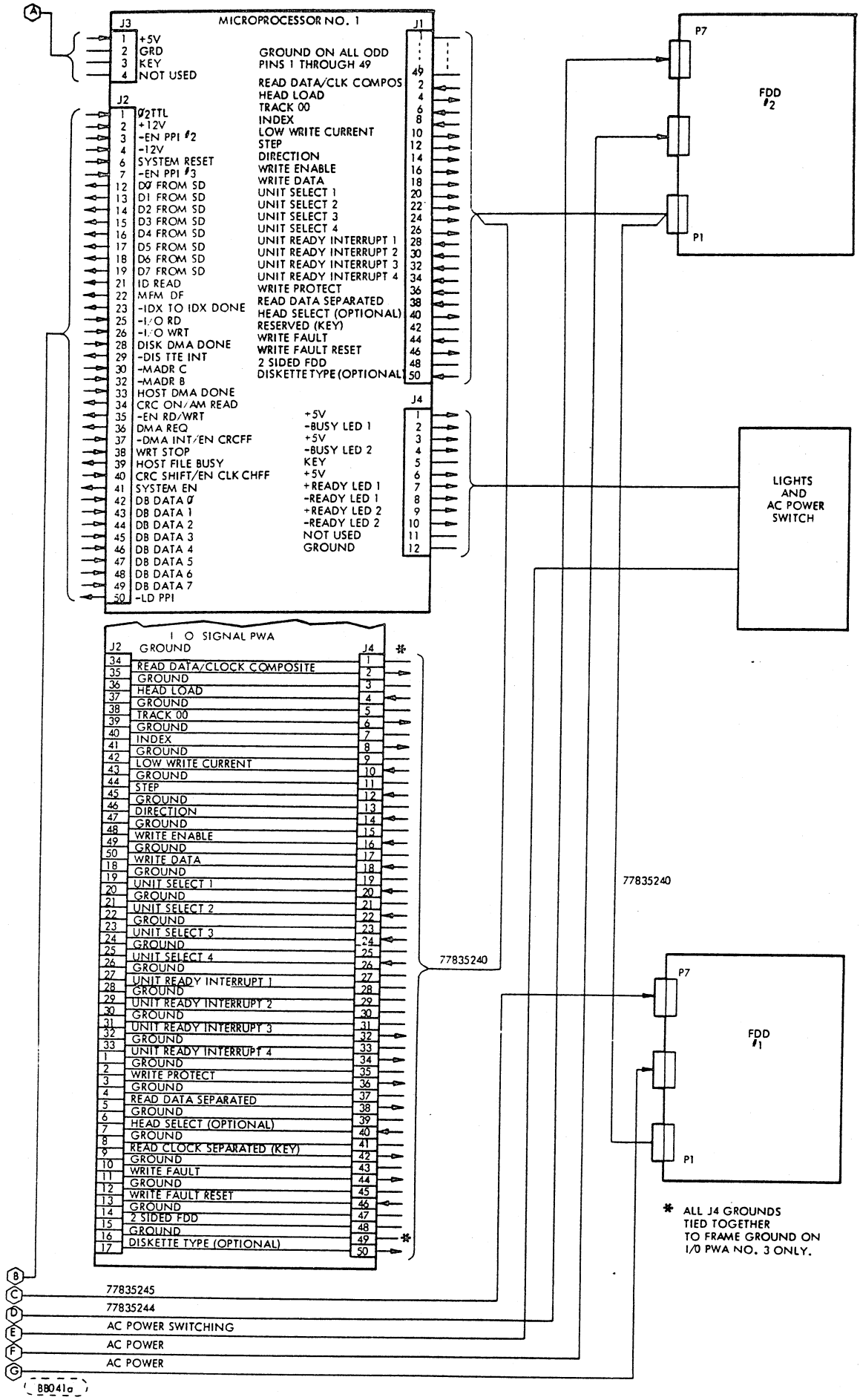


Figure 5-1. Interconnection Diagram (Master) - (Sheet 2 of 2)

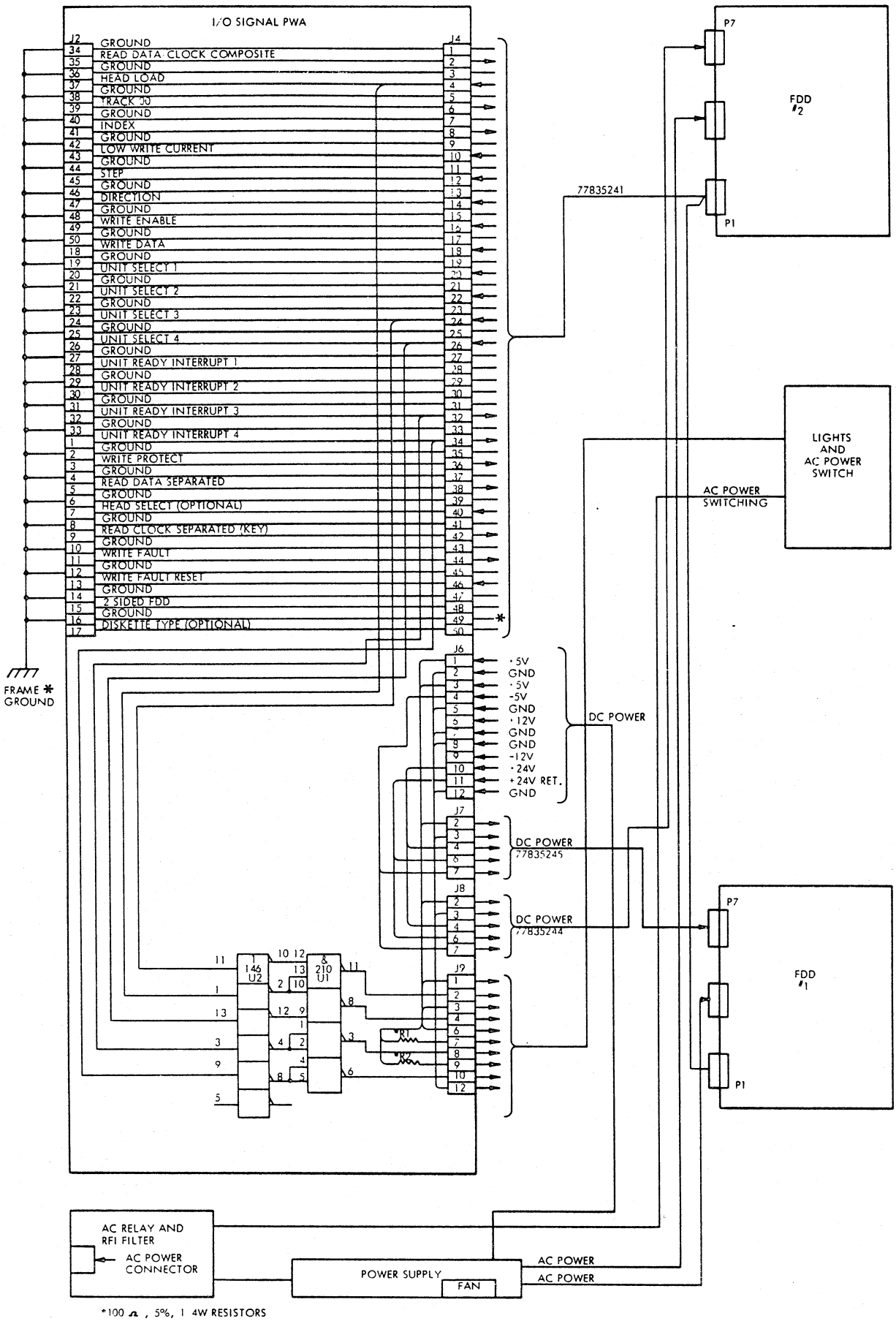


Figure 5-2. Interconnection Diagram (Slave)

5.4 LOGIC DIAGRAM SYMBOLOGY

5.4.1 GENERAL INFORMATION

Logic symbols are drawn with inputs on the left and outputs on the right whenever space and layout permit.

Power supply connections, discrete timing components, etc., may be shown connected to the top or bottom of the symbol. Unused pins and unused elements need not be shown. Figure 5-2 illustrates functionally equivalent symbols.

5.4.2 GENERAL SIGNAL ANNOTATION

S = Set input to bistable device.

R = Reset (Clear) input to bistable device.

G = Gate input has no direct action on circuit, but must be present before inputs (and/or outputs) are able to function. If more than one gate is used a numeric suffix is added (G1, G2, etc.).

D = Identifies a signal which requires the presence of another signal to perform its function.

C = Strobe pulse. Usually used to gate "D" inputs into a bistable device.

T = Toggle input. Bistable device changes state each time "T" assumes its specified state.

J = J output conditioned by leading edge of dynamic toggle (G).

K = K output conditioned by leading edge of dynamic toggle (G).

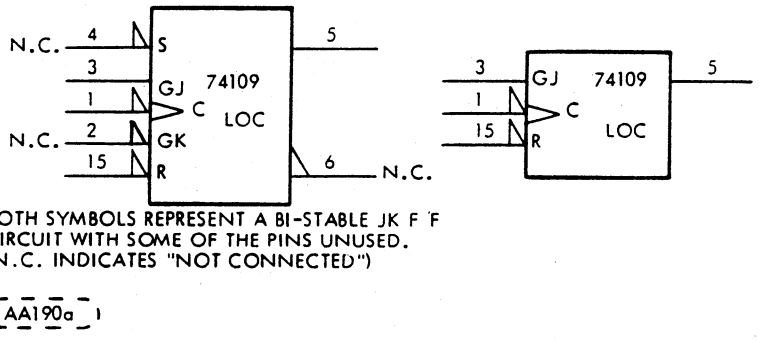
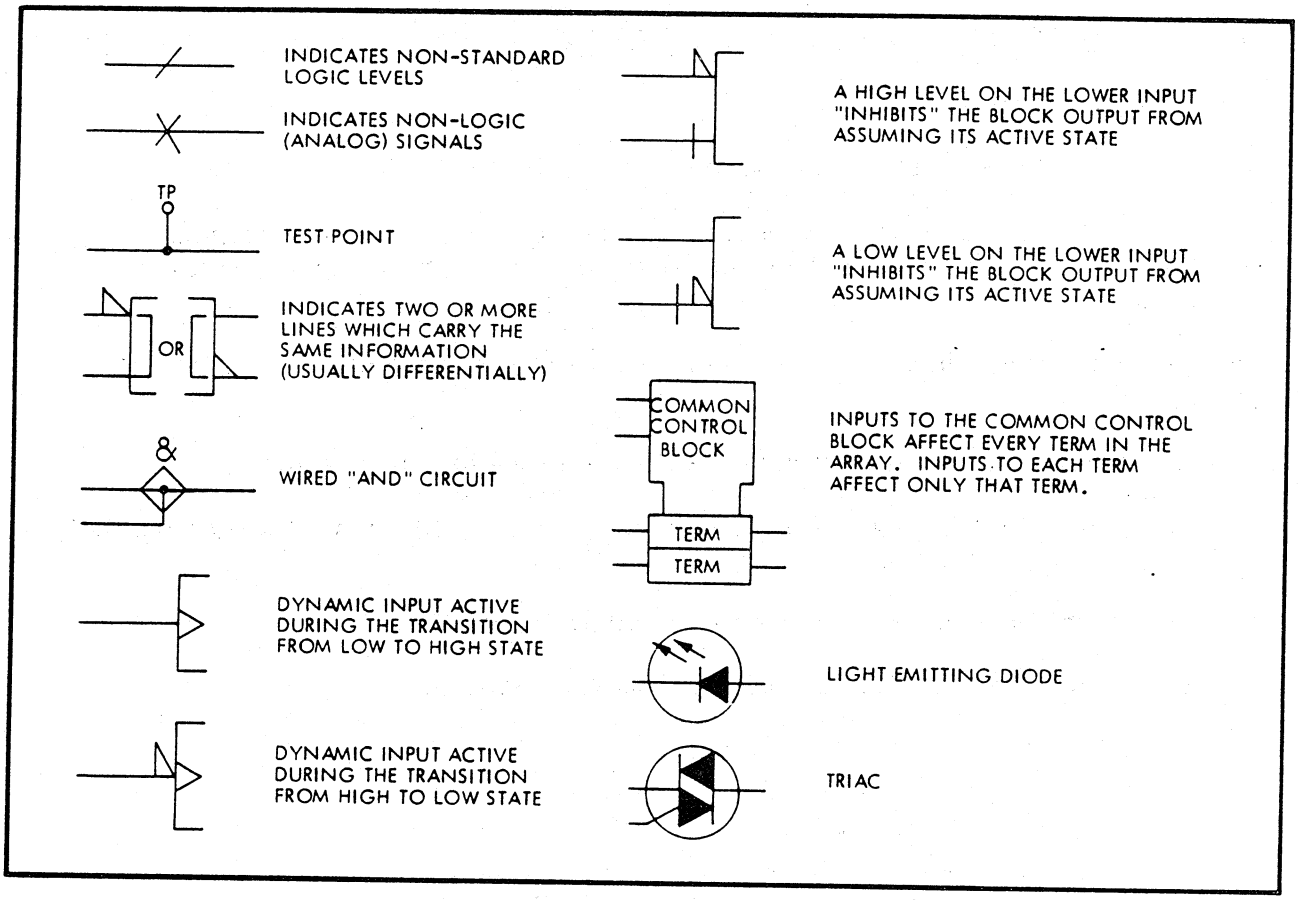


Figure 5-3. Functionally Equivalent Symbols

5.4.3 SYMBOLOGY

Logic Symbols are as described in Table 5-1.

Table 5-1. Logic Symbology

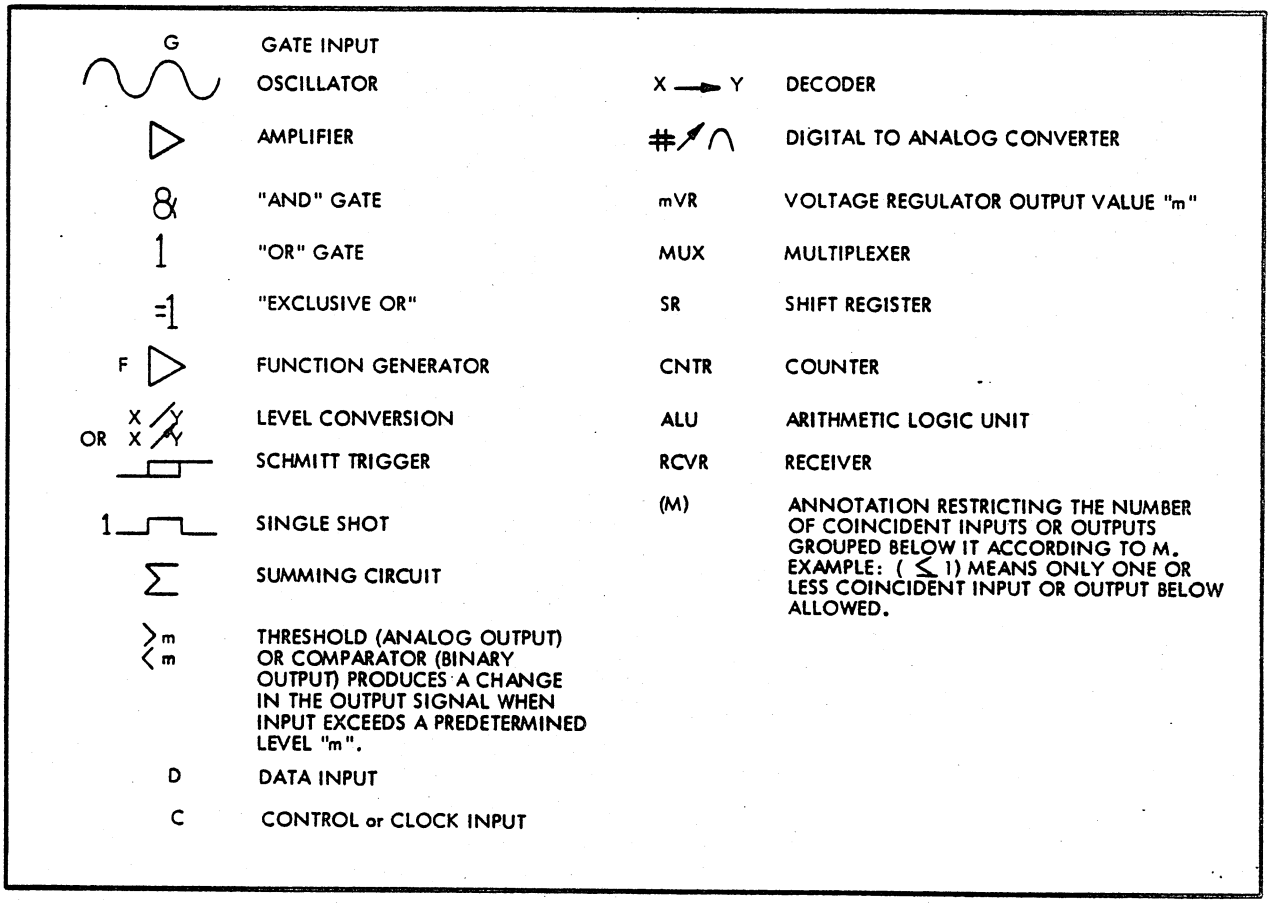


(AA142c)

5.4.4 FUNCTION SYMBOLOGY

Function symbols are as described in Table 5-2.

Table 5-2. Function Symbols



(AA142d)

5.4.5 ABBREVIATIONS

ACK = ACKNOWLEDGE

ADR = ADDRESS

AM = ADDRESS MARK

AMP = AMPLIFIER

CART = CARTRIDGE

CRC = CYCLIC REDUNDANCY CODE

CLK = CLOCK

CLR = CLEAR

CTL = CONTROL

CNT = COUNT

COM = COMMON

CUR = CURRENT

CYL = CYLINDER

D.F. = DOUBLE FREQUENCY (DATA)

DIFF = DIFFERENCE

DLY = DELAY

DMA = DIRECT MEMORY ACCESS

E = ERASE

EN = ENABLE

EOT = END OF TRAVEL

FF = FLIP-FLOP

FLT = FAULT

FWD = FORWARD

HD = HEAD

HLDA = HOLD ACKNOWLEDGE

INT = INTERRUPT

ID = IDENTIFICATION

IDX = INDEX

IO = INPUT/OUTPUT

LD = LOAD

MADR = MEMORY ADDRESS

MFM = MODIFIED FREQUENCY MODULATION (RECORDING TECHNIQUE)

M.P. = MICROPROCESSOR

NC = NORMALLY CLOSED

NO = NORMALLY OPEN

NRZ = NON RETURN TO ZERO

PATT = PATTERN

P.P.I. = PROGRAMMABLE PERIPHERAL INTERFACE

PWR = POWER

RCVR = RECEIVER

RDT = REQUEST FOR DATA TRANSFER

RDY = READY

R = READ

RD = READ

REV = REVERSE

RST = RESET

RTZS = RETURN TO ZERO SEEK

SC =

SEL = SELECT

T = TRACK

T.A. = TRACK ADDRESS

UDCTR = UP/DOWN COUNTER

UNSEP = UNSEPARATED

VEL = VELOCITY

VFO = VARIABLE FREQ. OSCILLATOR

W = WRITE

WRT = WRITE

5.4.6 IC INDEX AND CROSS REFERENCE

Refer to Table 5-3 for a cross reference between element number and manufacturer type.

Table 5-3. Integrated Circuit Index and Cross Reference

ELEMENT	PART NO.	TYPE	FUNCTION
140	3186800	7400	TTL QUAD 2-INPUT NAND
140LS	15144900	74LS00	TTL QUAD 2-INPUT NAND
141	50250700	7410	TTL TRIPLE 3-INPUT NAND
145	3618700	7450	TTL DUAL 2 WIDE 2-IN AND-OR-INVERT
146	36187100	7404	TTL HEX INVERTER
146LS	15145100	74LS04	TTL HEX INVERTER
148	36187000	7402	TTL QUAD 2-INPUT NOR
158LS	15146800	74LS161	COUNTER, TTL 4 BIT BINARY
175	15104800	7474	TTL DUAL D-TYPE F/F
189	51784000	74157	MULTIPLEXER TTL QUAD 2-INPUT
195	15104301	9602	MULTIVIBRATOR, DUAL RETRIGGERABLE TTL
195S	15154400	AM 26S02	MULTIVIBRATOR, DUAL RETRIGGERABLE TTL
201	51801200	7408	TTL QUAD 2-INPUT NAND
204	15158300	7438	TTL QUAD 2-INPUT NAND BUFFER (OC)
208	36187300	7420	TTL DUAL 4-INPUT NAND
210	15107000	7437	TTL QUAD 2-INPUT NAND BUFFER
213	15129700	7411	TTL TRIPLE 3-INPUT AND
218	15114700	7432	TTL QUAD 2-INPUT OR
243S	15109400	74S112	TTL DUAL J-K F/F
296	94684200	7400	TTL QUAD 2-INPUT NAND
297	94684201	7410	TTL TRIPLE 3-INPUT NAND
301	50251300	741C	OPERATIONAL AMPL.
340	15125500	741C	OPERATIONAL AMPL.
500	17184200	74193	COUNTER, TTL 4-BIT BINARY UP-DOWN
507	36187600	7442A	DECODER, TTL BCD-TO-DECIMAL (1 OF 10)
527	15109900	74164	COUNTER TTL 4 BIT BINARY
544	15148300	74LS279	LATCH, QUAD S-R
558	15138300	8080A	PROCESSOR UNIT, MOS 8-BIT
582	15105700	MC4024	MULTIVIBRATOR, DUAL VOLTAGE CONT.
780	15151600	8111-A	MEMORY, MOS 256X4 RAM
901A	36186501	MC1489A	RECEIVER, RS-232C TO DTL QUAD LINE
930	15113000	75452	DRIVER, DUAL PERIPHERAL NAND
939	15140400	8097	DRIVER, TTL HEX TRI-STATE
150	51761500	74161	COUNTER, TTL 4-BIT BINARY
573	15153400	8228	SYSTEM CONTROL & BUS DRIVER FOR 8080
574	15153300	8255	PROGRAMMABLE PERIPHERAL INTERFACE
576	15153500	8224	CLOCK GENERATOR/DRIVER FOR 8080
	15155400	8212	I/O PORT, 8-BIT PARALLEL
	15157300	8506	CRC GENERATOR/CHECKER
781	15153900*	2708	1024X8 EPROM (Unprogrammed)
552	15106900	9334	LATCH, TTL 8-BIT
	15160200	8257	DMA/PERIPHERAL CONTROLLER
240LS	15148000	74LS109	TTL DUAL J-K F/F
543	15131800	74199	8 BIT SHIFT REGISTER

*See Parts List of Figure 5-5 for Programmed Part Numbers.

5.5 DIAGRAMS AND PWA PARTS LISTS

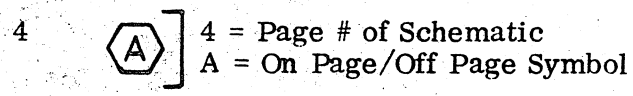
This Section contains schematic diagrams, part placement drawings and parts lists for the printed wiring boards, as well as power system AC interconnections and power supply internal interconnection diagrams.

5.5.1 USE OF SCHEMATIC DIAGRAMS

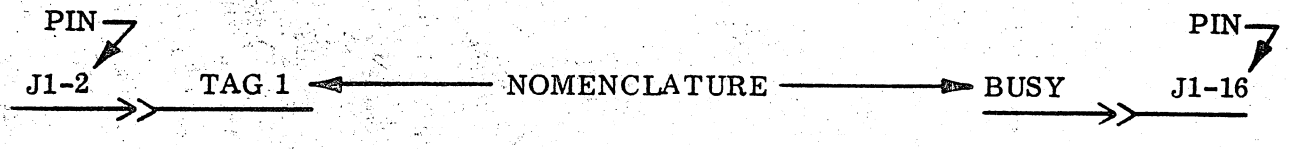
Multiple page (set of pages) circuit board electrical schematics are sequentially numbered (①, ②, ③, etc.) in the upper right-hand corner of each schematic page. Off-page/On-page number references on the face of the schematics apply only to the pages in the set (Schematic, PL and Assembly).

Connector diagrams, Figures 5-1 and 5-2, provide the cross reference data necessary to trace signals from one board to another.

SYMBOL (INTERBOARD CONNECTIONS)



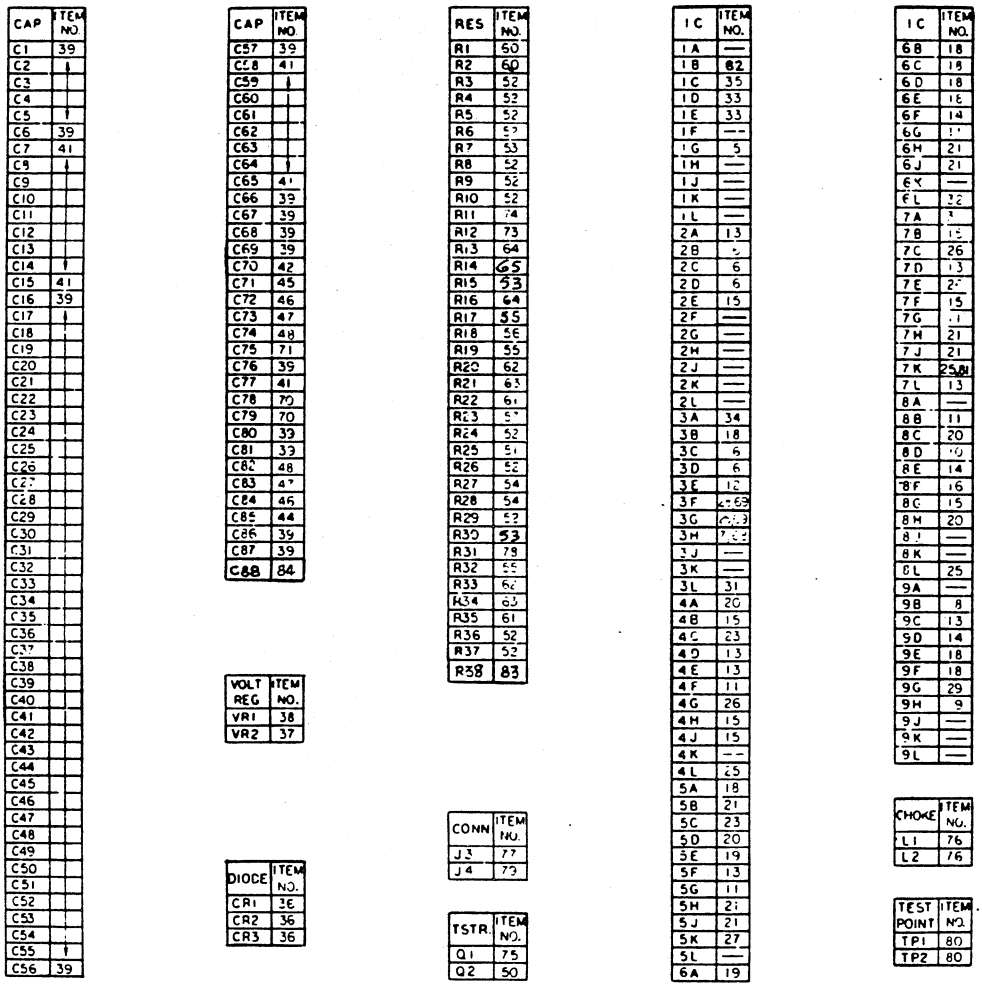
BOARD TO BOARD CONNECTIONS



The direction the arrows are pointing on the connector diagrams indicate sourve of signal.

5.5.2 LOCATING PARTS

On the board layout drawings (Sheet 2) the resistors, capacitors diodes and connectors are labeled R1, C1, D1 and etc. The table (Sheet 2) lists the correspondence between these numbers and the item number on the parts list (Sheets 3 and 4). For integrated circuits (ICs) the board is divided into coordinates with A through L along one side and 1 through 9 along the other side. For example, item 28 on the parts list (an 8255 PPI circuit) is found at board grid location 3F.



CAP	ITEM NO.
C1	39
C2	↓
C3	
C4	
C5	↑
C6	39
C7	41
C8	↓
C9	
C10	
C11	
C12	
C13	
C14	↑
C15	41
C16	39
C17	↓
C18	
C19	
C20	
C21	
C22	
C23	
C24	
C25	
C26	
C27	
C28	
C29	
C30	
C31	
C32	
C33	
C34	
C35	
C36	
C37	
C38	
C39	
C40	
C41	
C42	
C43	
C44	
C45	
C46	
C47	
C48	
C49	
C50	
C51	
C52	
C53	
C54	
C55	↑
C56	39

CAP	ITEM NO.
C57	39
C58	41
C59	↓
C60	
C61	
C62	
C63	
C64	↑
C65	41
C66	39
C67	39
C68	39
C69	39
C70	42
C71	45
C72	46
C73	47
C74	48
C75	71
C76	39
C77	41
C78	70
C79	70
C80	39
C81	39
C82	48
C83	47
C84	46
C85	44
C86	39
C87	39
C88	84

VOLT REG	ITEM NO.
VR1	38
VR2	37

DIODE	ITEM NO.
CR1	36
CR2	36
CR3	36

RES	ITEM NO.
R1	60
R2	60
R3	52
R4	52
R5	52
R6	52
R7	53
R8	52
R9	52
R10	52
R11	74
R12	73
R13	64
R14	65
R15	53
R16	64
R17	55
R18	56
R19	55
R20	62
R21	63
R22	61
R23	57
R24	52
R25	51
R26	52
R27	54
R28	54
R29	52
R30	53
R31	78
R32	55
R33	62
R34	63
R35	61
R36	52
R37	52
R38	83

CONN	ITEM NO.
J3	77
J4	79

TSTR.	ITEM NO.
Q1	75
Q2	50

IC	ITEM NO.
1A	—
1B	82
1C	35
1D	33
1E	33
1F	—
1G	5
1H	—
1J	—
1K	—
1L	—
2A	13
2B	6
2C	6
2D	6
2E	15
2F	—
2G	—
2H	—
2J	—
2K	—
2L	—
3A	34
3B	18
3C	6
3D	6
3E	12
3F	68
3G	69
3H	69
3J	—
3K	—
3L	31
4A	20
4B	15
4C	23
4D	13
4E	13
4F	11
4G	26
4H	15
4J	15
4K	—
4L	25
5A	18
5B	21
5C	23
5D	20
5E	19
5F	13
5G	11
5H	21
5J	21
5K	27
5L	—
6A	19

IC	ITEM NO.
6B	18
6C	18
6D	18
6E	18
6F	14
6G	11
6H	21
6J	21
6K	—
6L	32
7A	3
7B	12
7C	26
7D	13
7E	27
7F	15
7G	11
7H	21
7J	21
7K	25
7L	13
8A	—
8B	11
8C	20
8D	10
8E	14
8F	16
8G	15
8H	20
8J	—
8K	—
8L	25
9A	—
9B	8
9C	13
9D	14
9E	18
9F	18
9G	29
9H	9
9J	—
9K	—
9L	—

CHOKE	ITEM NO.
L1	76
L2	76

TEST POINT	ITEM NO.
TP1	80
TP2	80

Figure 5-4. PWA Microprocessor No. 1 - (Sheet 1 of 15)

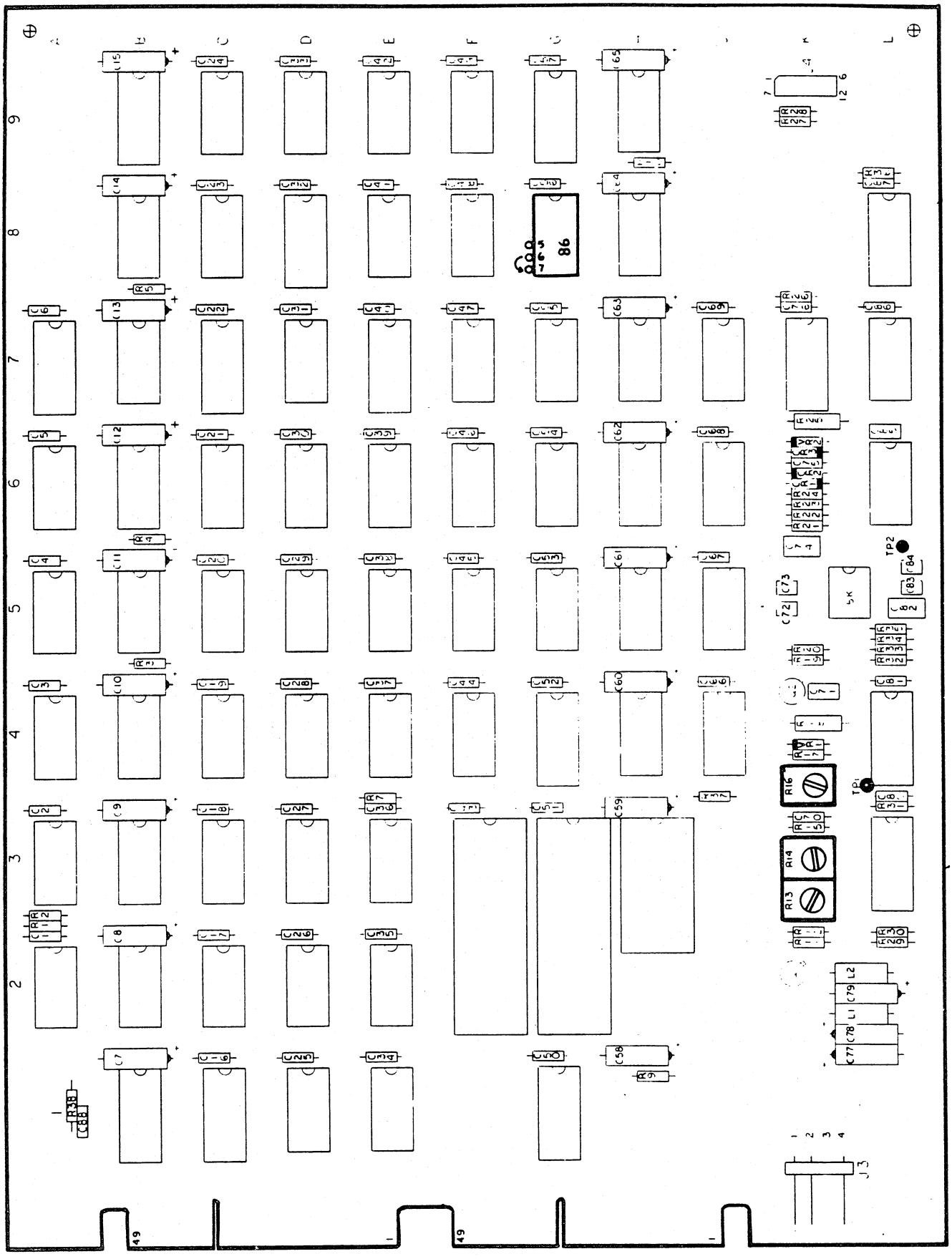


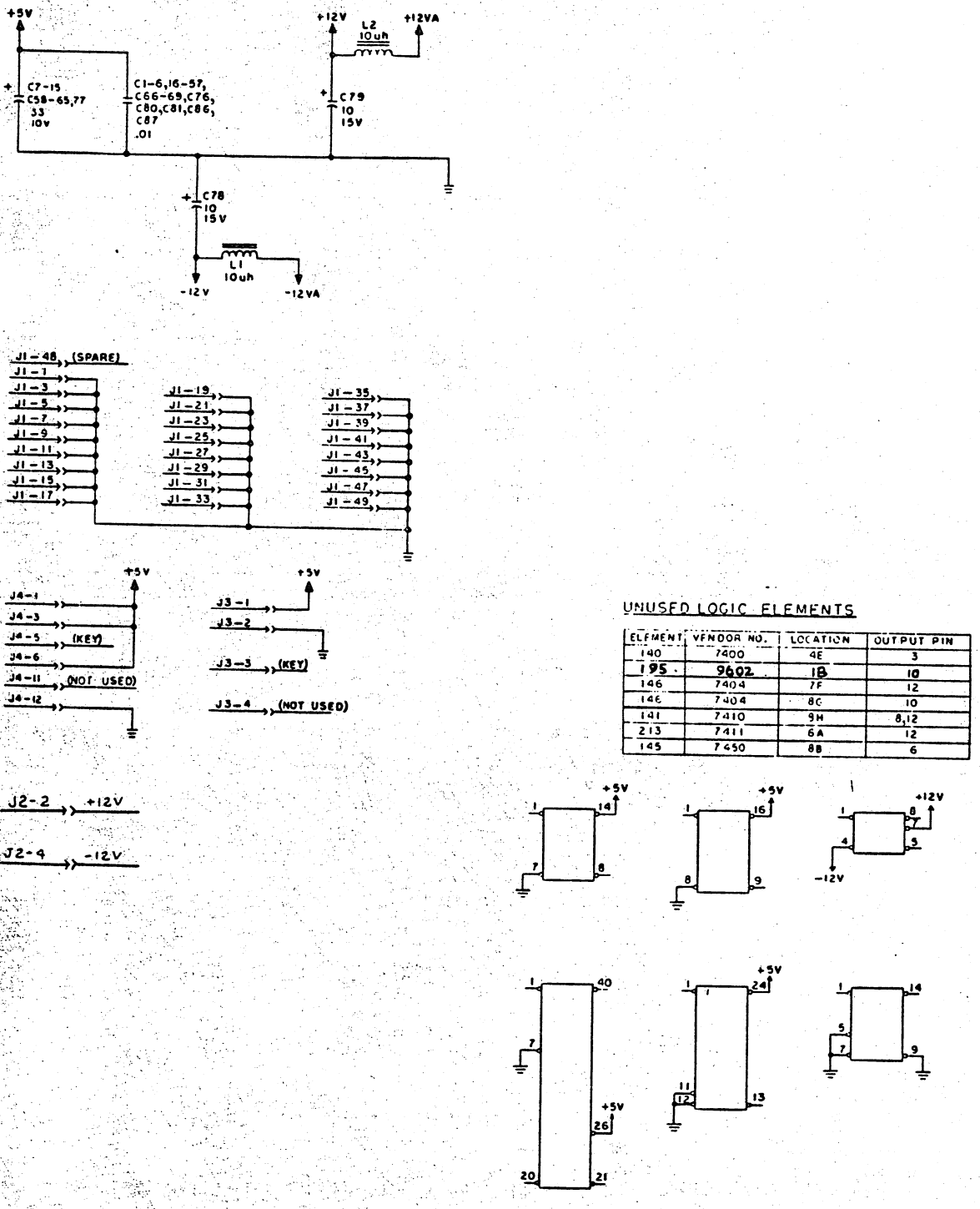
Figure 5-4. PWA Microprocessor No. 1 - (Sheet 2 of 15)

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	75896500-8	PWA Micro Processor No. 1	Used on 75897100-6
2	75896520-6	PWB Micro Processor No. 1	
5	15148300-5	I.C. 74LS279	
6	15107000-0	I.C. 7437	
7	15131800-3	I.C. 74199	
8	15146800-6	I.C. 74LS161	
9	15109900-9	I.C. 74164	
10	51761500-1	I.C. 74161	
11	36187700-4	I.C. 7450	
12	15145100-2	I.C. 74LS04	
13	66299099-3	I.C. 7400	
14	88897000-1	I.C. 7408	
15	39389700-4	I.C. 7404	
16	15114700-6	I.C. 7432	
18	96744156-9	I.C. 7474	
19	15129700-9	I.C. 7411	
20	66299100-9	I.C. 7410	
21	36187400-1	I.C. 7430	
23	36187300-3	I.C. 7420	
25	15158600-5	I.C. 74S112	
26	15148000-1	I.C. 74LS109	
27	15125500-7	I.C. 741C	
28	15153300-7	I.C. 8255	
29	15157300-3	I.C. 8506	
30	51784000-5	I.C. 74157/9322	
31	15164400-2	I.C. AM 26S02	
32	15105700-7	I.C. MC4024	
33	36186501-7	I.C. MC1489A	
34	77834362-4	Delay Line	
35	95894500-8	Res Pac 220/330	
36	83432400-6	Diode	
37	50240107-8	Volt Reg 5.6V 5%	
38	50240108-6	Volt Reg 6.2V 5%	
39	92496227-7	Cap 100V 20% .01 uF	
41	24504353-4	Cap 10V 20% 33 uF	
42	94240423-7	Cap 50V 10% 150 pF	
44	94227227-9	Cap 300V 2% 110 pF	
45	94354817-2	Cap 50V 20% .47 uF	
46	94354806-5	Cap 50V 20% .10 uF	
47	94354804-0	Cap 50V 20% .047 uF	
48	94227253-5	Cap 100V 2% 1300 pF	
50	75722200-5	Transistor NPN	
51	24500144-1	Res 1/2W 5% 160	

Figure 5-4. PWA Microprocessor No. 1 - (Sheet 3 of 15)

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
52	24500063-3	Res 1/4W 5% 1K	
53	24500080-7	Res 1/4W 5% 5.1K	
54	24500039-3	Res 1/4W 5% 100	
55	24500071-6	Res 1/4W 5% 2.2K	
56	24500149-0	Res 1/2W 5% 270	
57	24500065-8	Res 1/4W 5% 1.2K	
60	94360258-1	Res 1/4W 1% 402	
61	94360304-3	Res 1/4W 1% 1.10K	
62	94360352-2	Res 1/4W 1% 3.48K	
63	94360400-9	Res 1/4W 1% 10.0K	
64	94372606-7	Res Vari 20% 10K	
65	94372607-5	Res Vari 20% 20K	
68	51358100-4	Socket 24 Pin	
69	51858103-8	Socket 40 Pin	
70	24504369-0	Cap 15V 20%10 uF	
71	92496215-2	Cap 100V 10% 1000	
73	94360287-0	Res 1/4W 1% 806	
74	94360214-4	Res 1/4W 1% 140	
75	16547200-2	Trans PNP 2N2907A	
76	94356324-7	Inductor 10 mH	
77	77600002-8	Right Angle Header	
78	24500059-1	Res 1/4W 5% 680	
79	83434505-0	Header, 12 Pin	
80	36185200-7	Turret-solid PWB	
81	94260301-0	Socket 16 Pin	
82	15104301-5	IC 9602	
83	94360393-6	Res, 1/4W, 1%, 9.31K	
84	94227218-8	Cap, 47 pF	

Figure 5-4. PWA Microprocessor No. 1 - (Sheet 4 of 15)



UNUSED LOGIC ELEMENTS

ELEMENT	VENDOR NO.	LOCATION	OUTPUT PIN
140	7400	4E	3
195	9602	1B	10
146	7404	7F	12
146	7404	8C	10
141	7410	9H	8,12
213	7411	6A	12
145	7450	8B	6

Figure 5-4. PWA Microprocessor No. 1 - (Sheet 5 of 15)

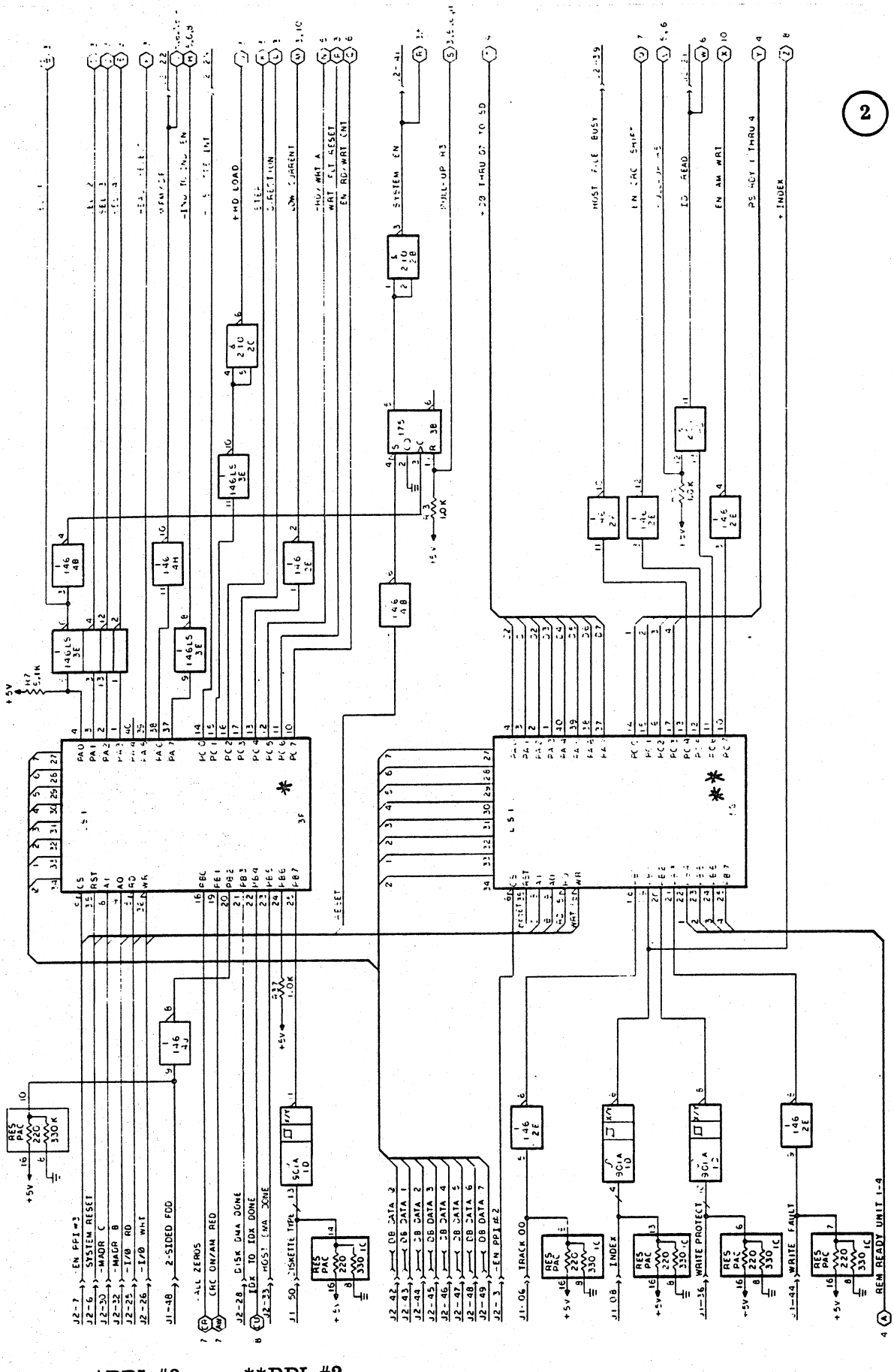


Figure 5-4. PWA Microprocessor No. 1 - (Sheet 6 of 15)

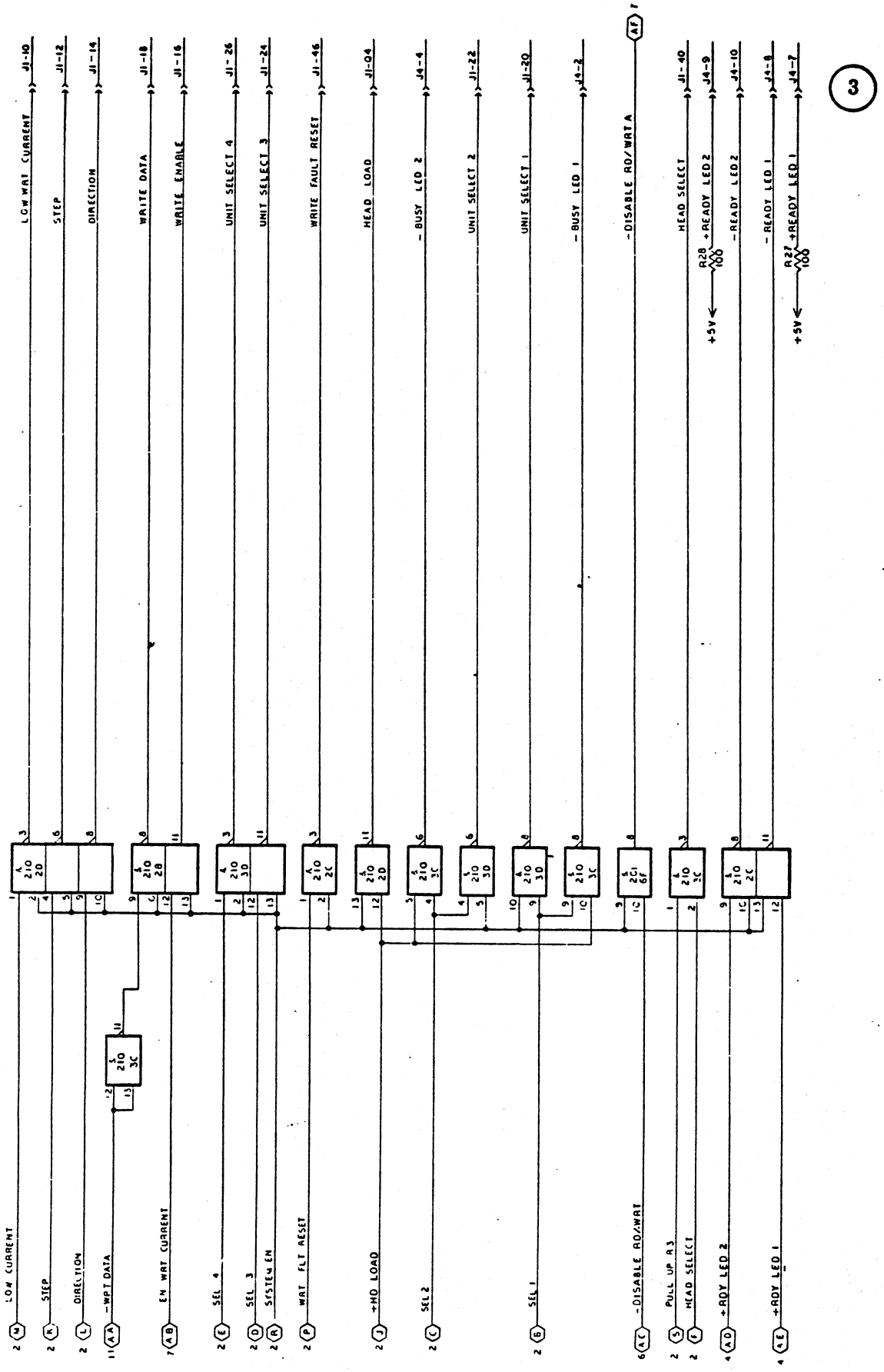


Figure 5-4. PWA Microprocessor No. 1 - (Sheet 7 of 15)

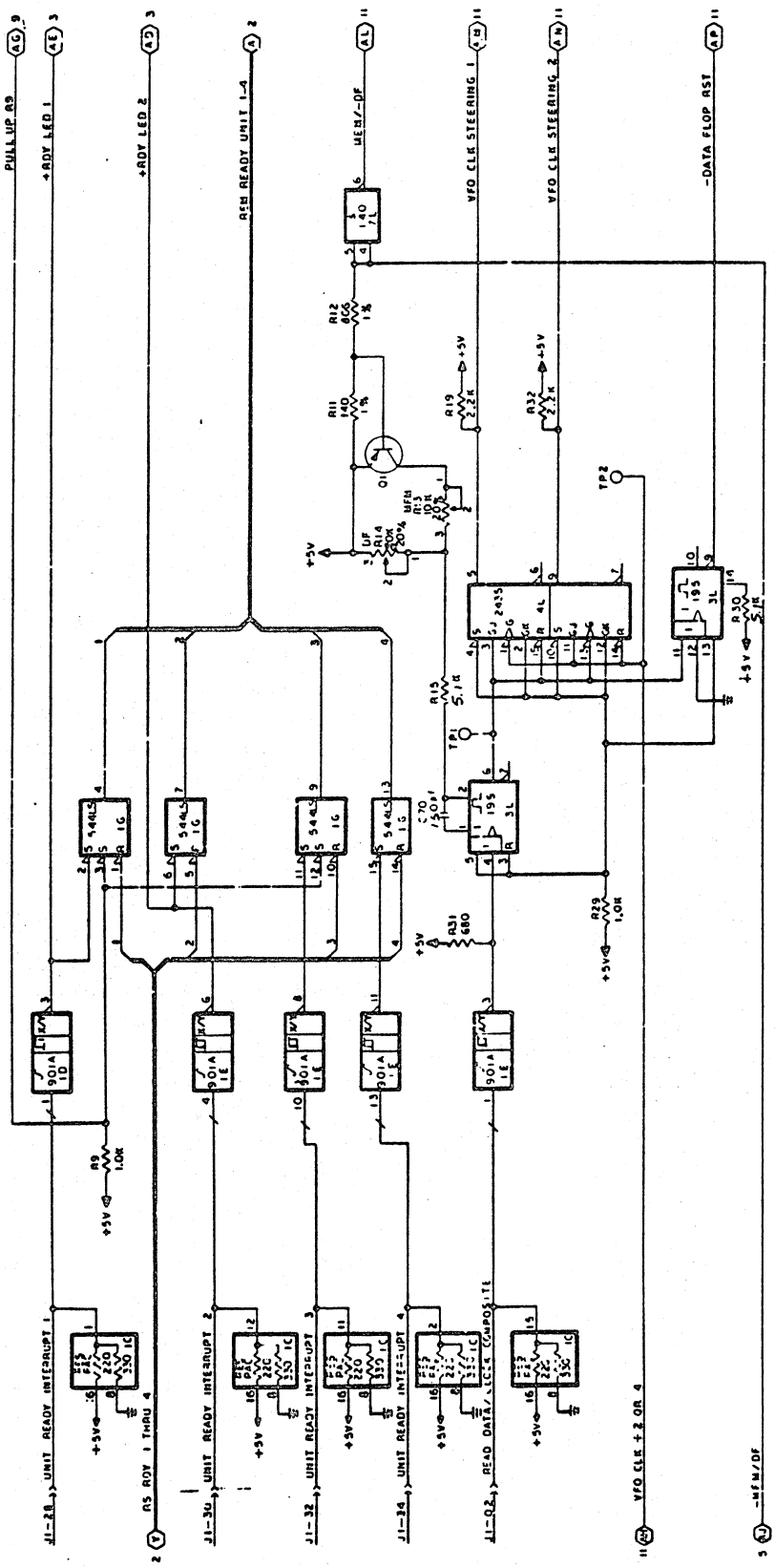


Figure 5-4. PWA Microprocessor No. 1 - (Sheet 8 of 15)

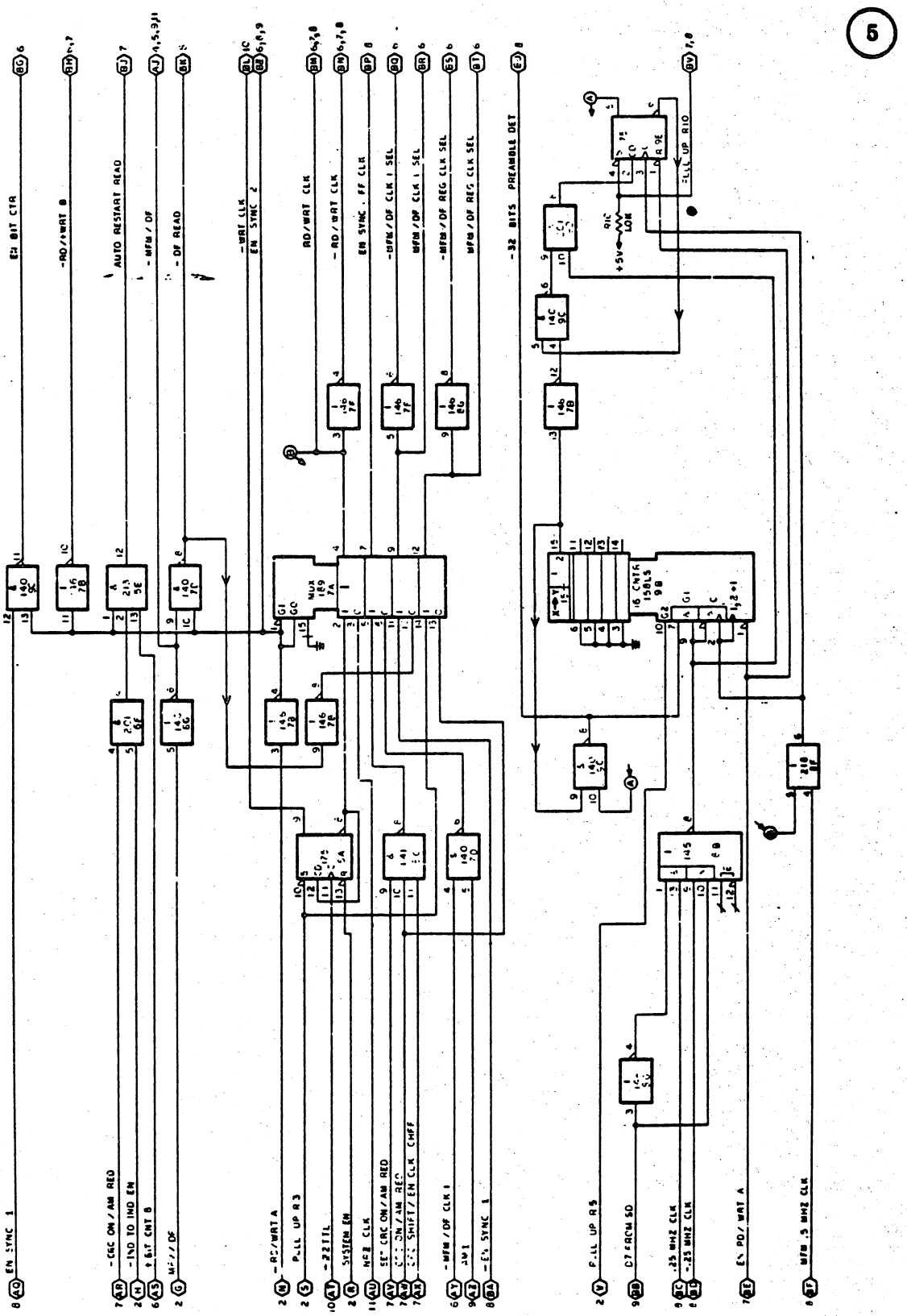


Figure 5-4. PWA Microprocessor No. 1 - (Sheet 9 of 15)

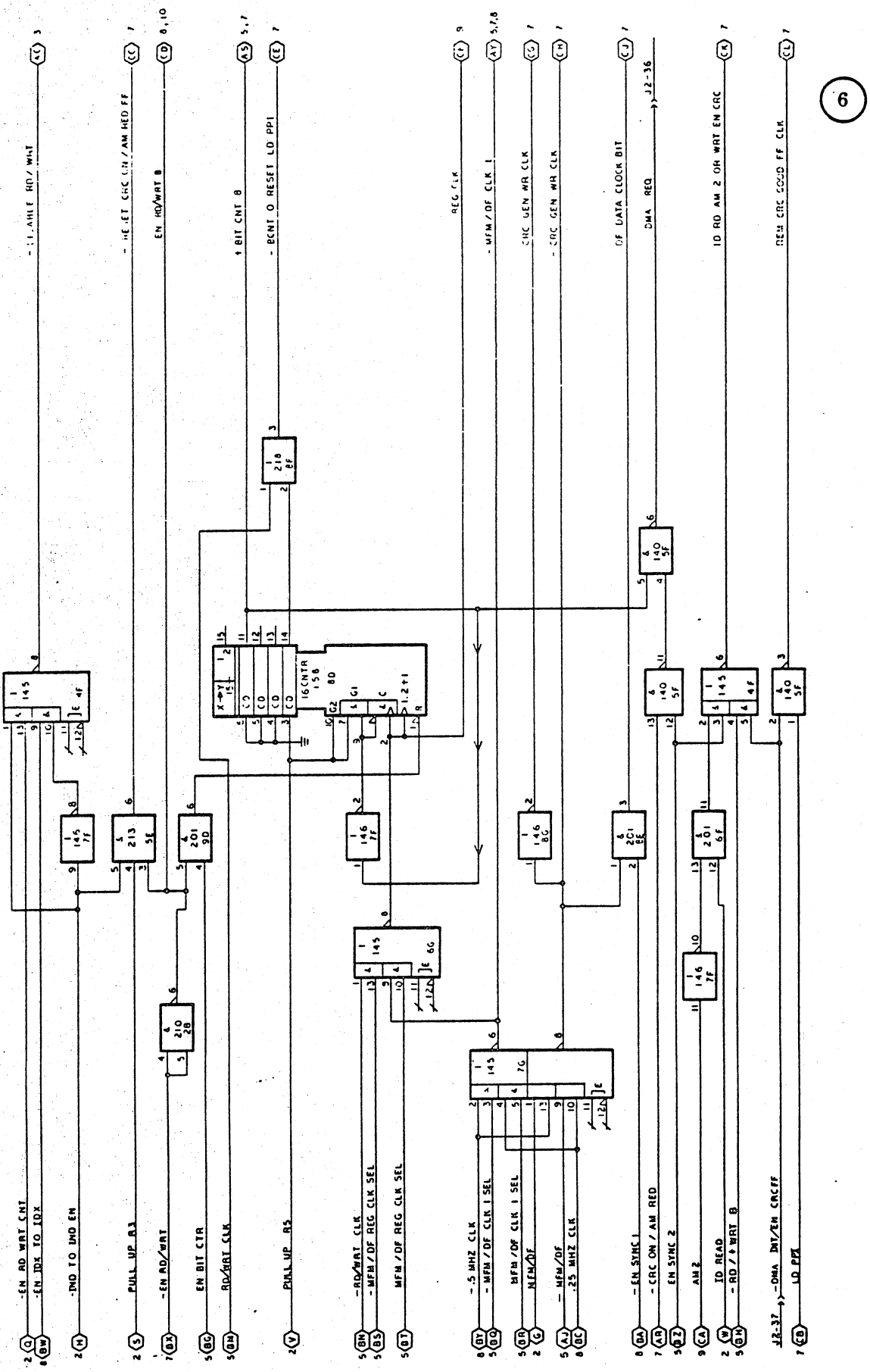


Figure 5-4. PWA Microprocessor No. 1 - (Sheet 10 of 15)

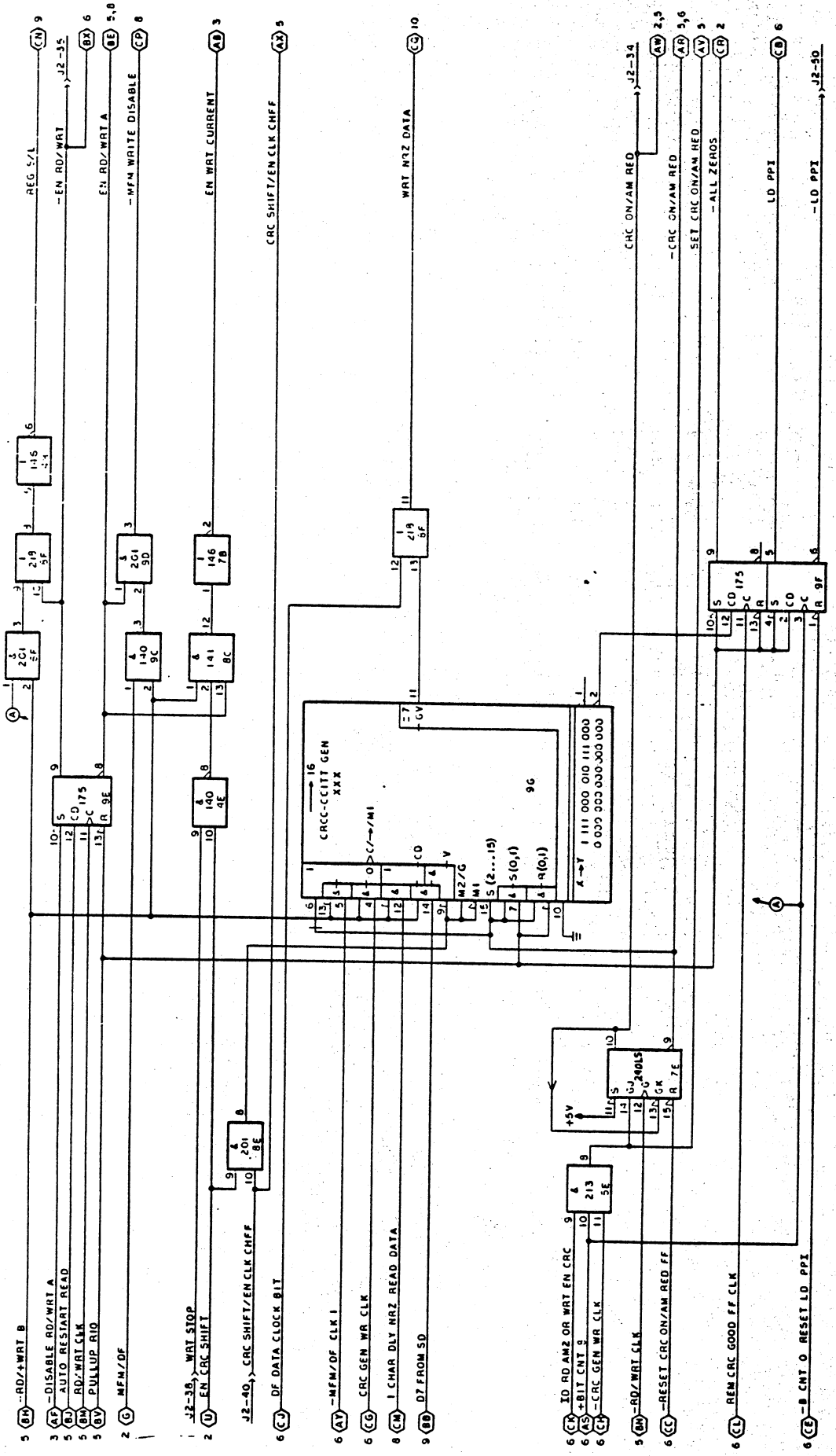


Figure 5-4. PWA Microprocessor No. 1 - (Sheet 11 of 15)

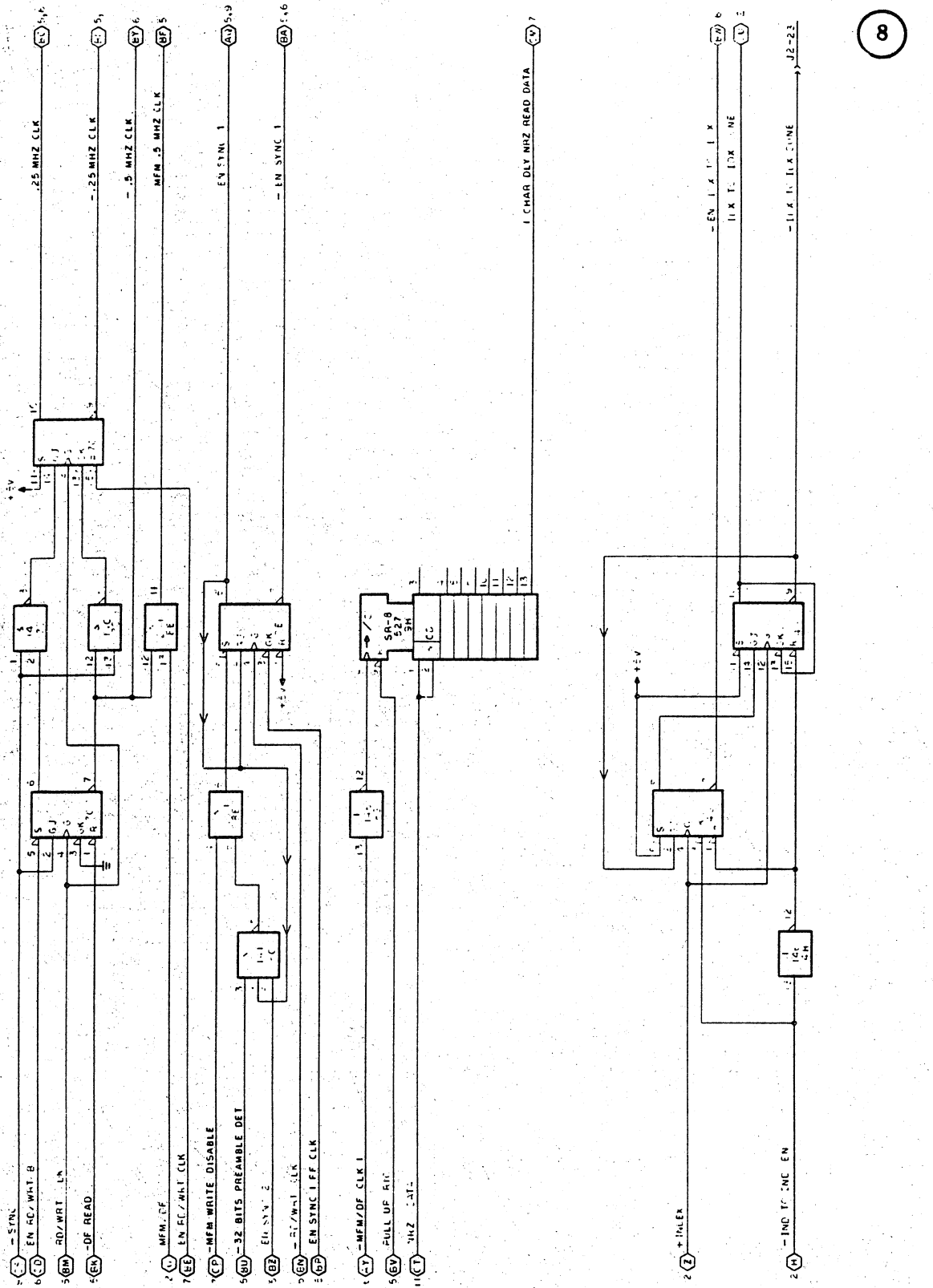


Figure 5-4. PWA Microprocessor No. 1 - (Sheet 12 of 15)

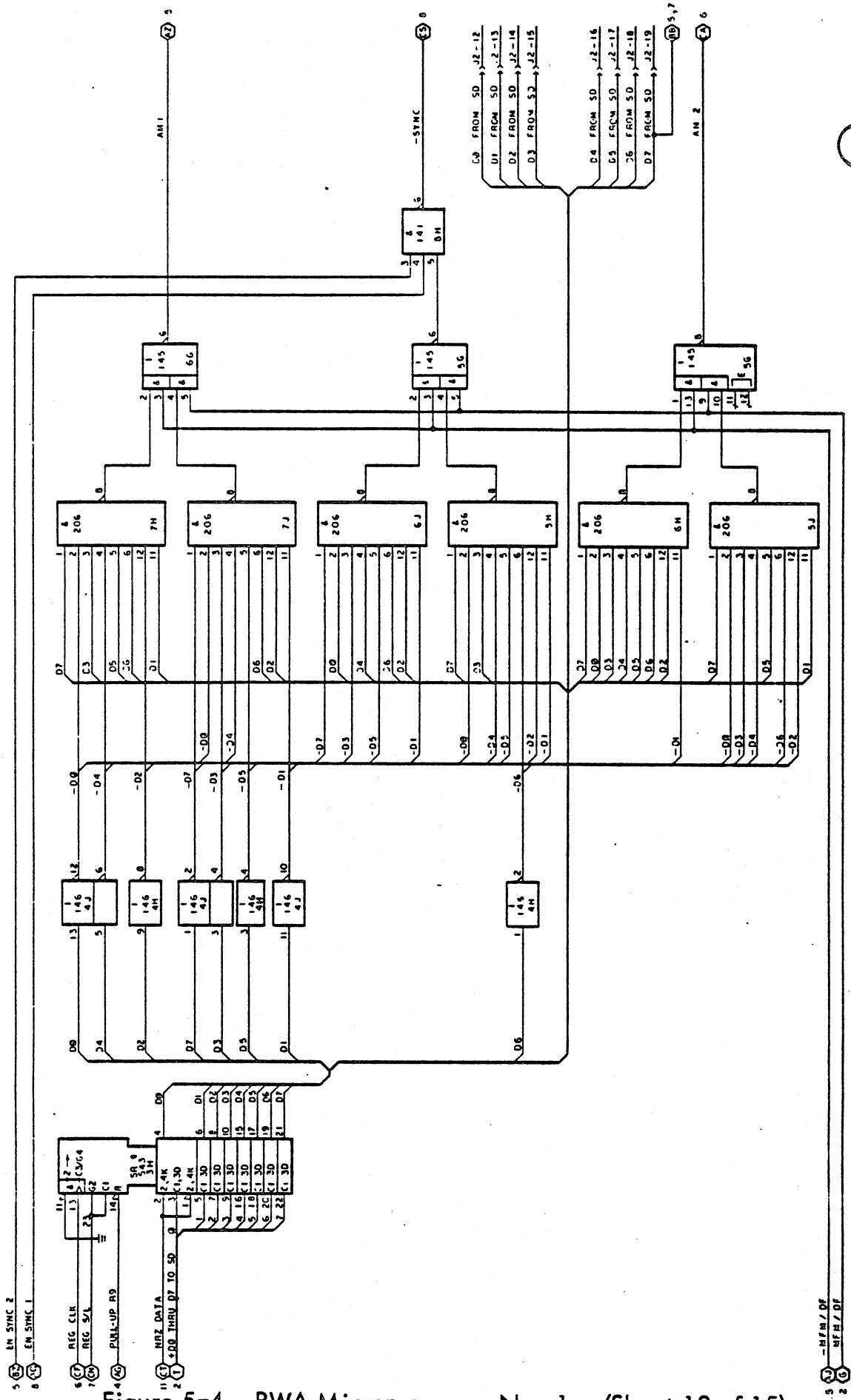


Figure 5-4. PWA Microprocessor No. 1 - (Sheet 13 of 15)

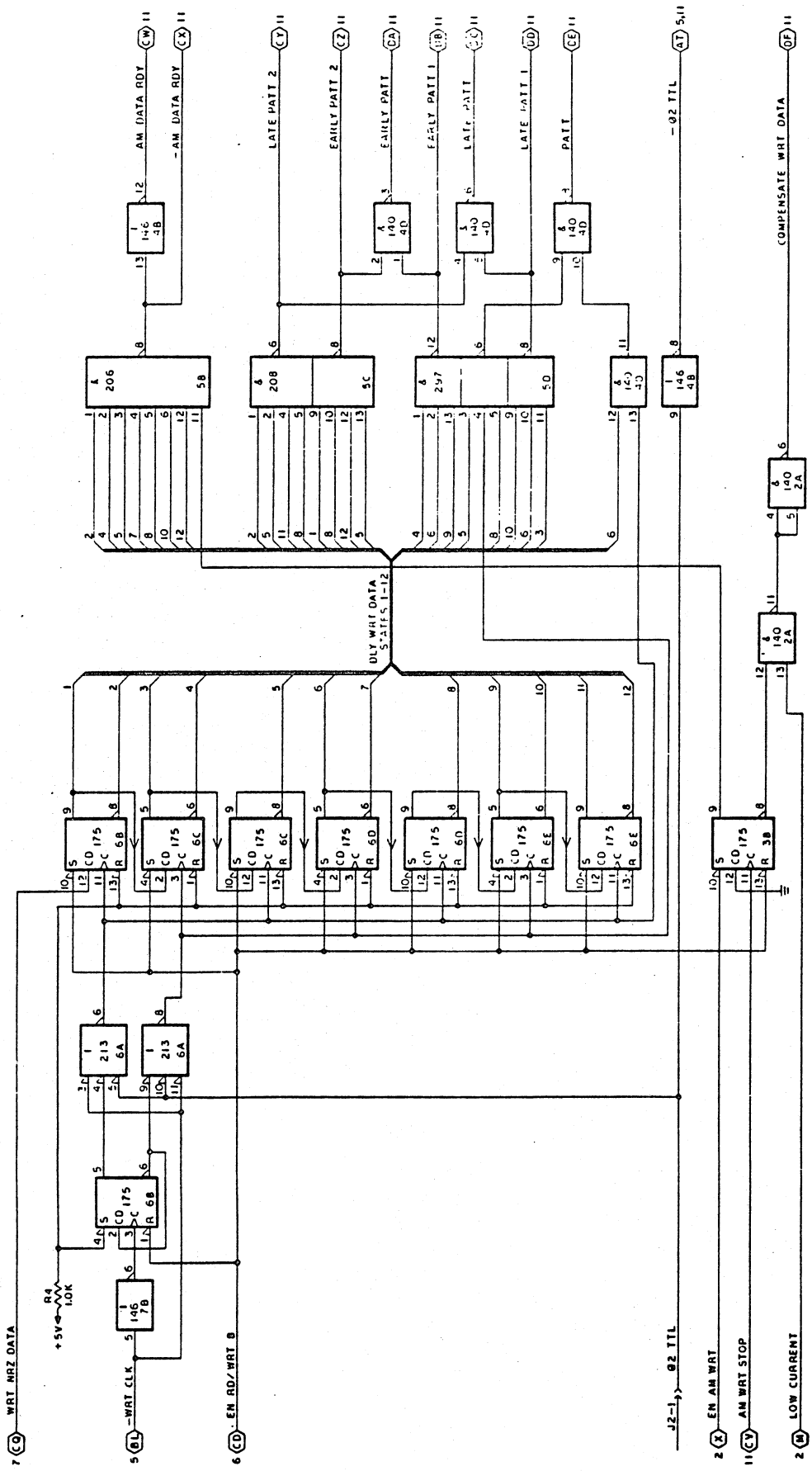


Figure 5-4. PWA Microprocessor No. 1 - (Sheet 14 of 15)

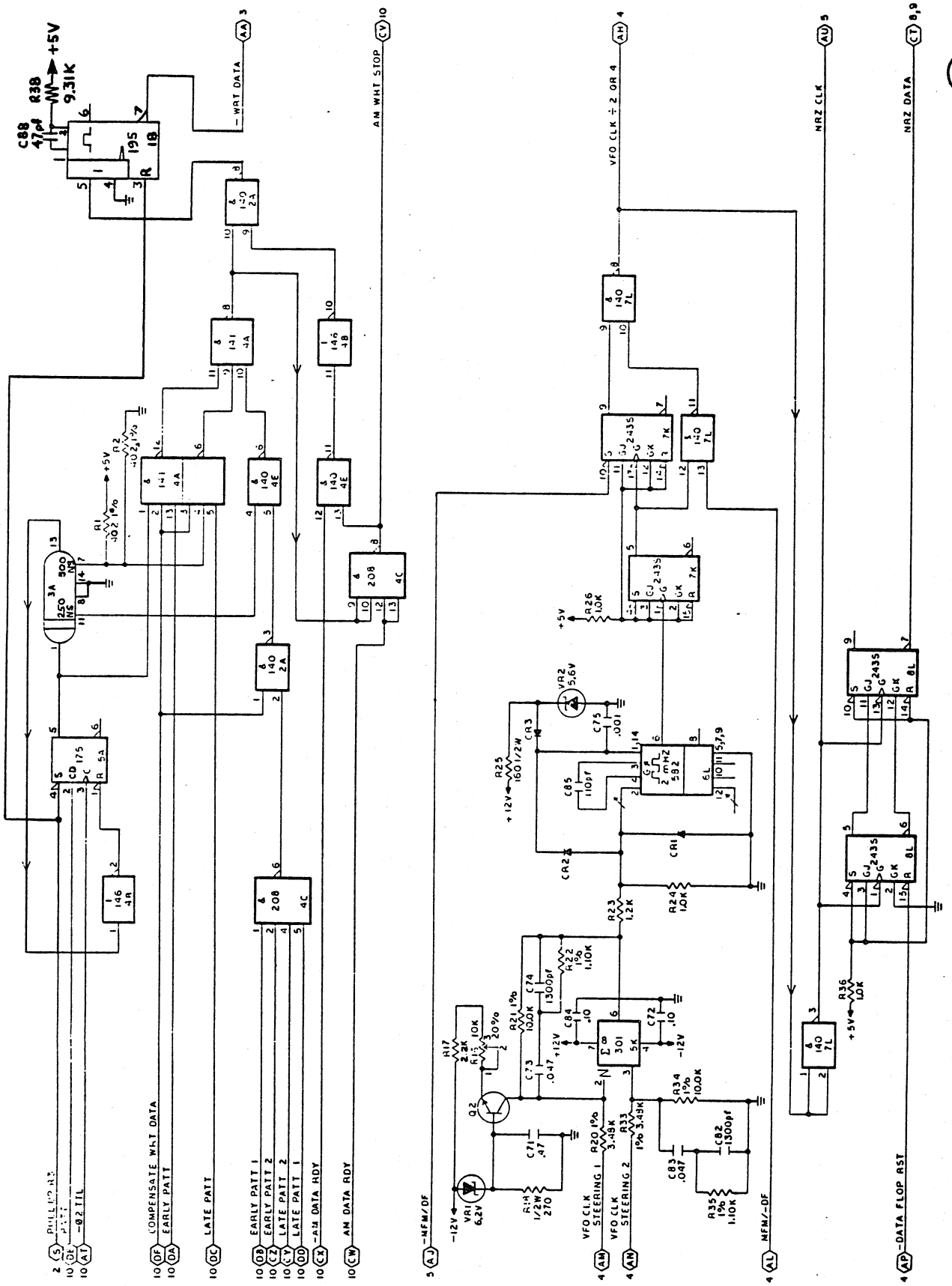


Figure 5-4. PWA Microprocessor No. 1 - (Sheet 15 of 15)

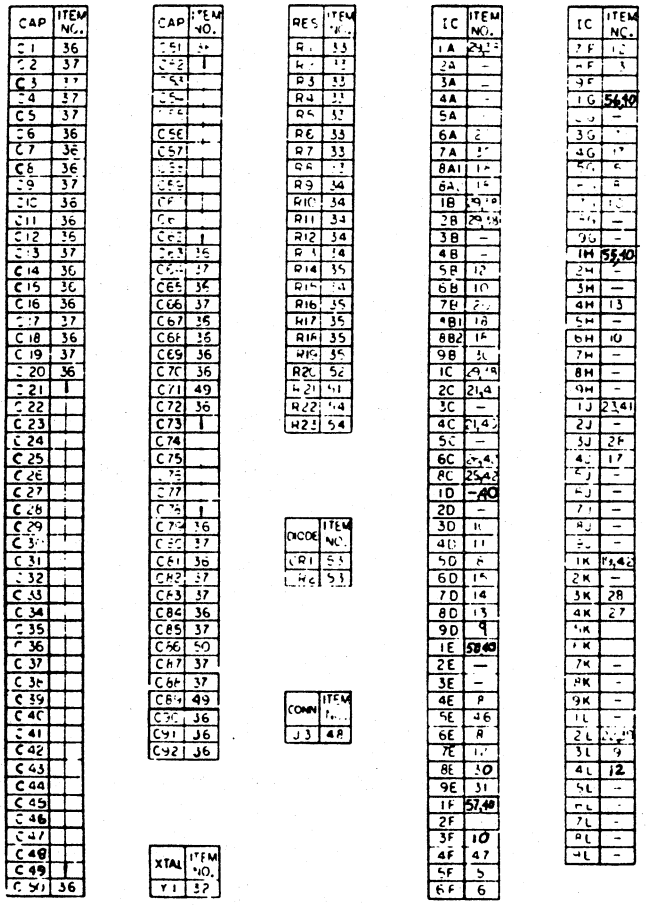


Figure 5-5. PWA Microprocessor No. 2 - (Sheet 1 of 11)

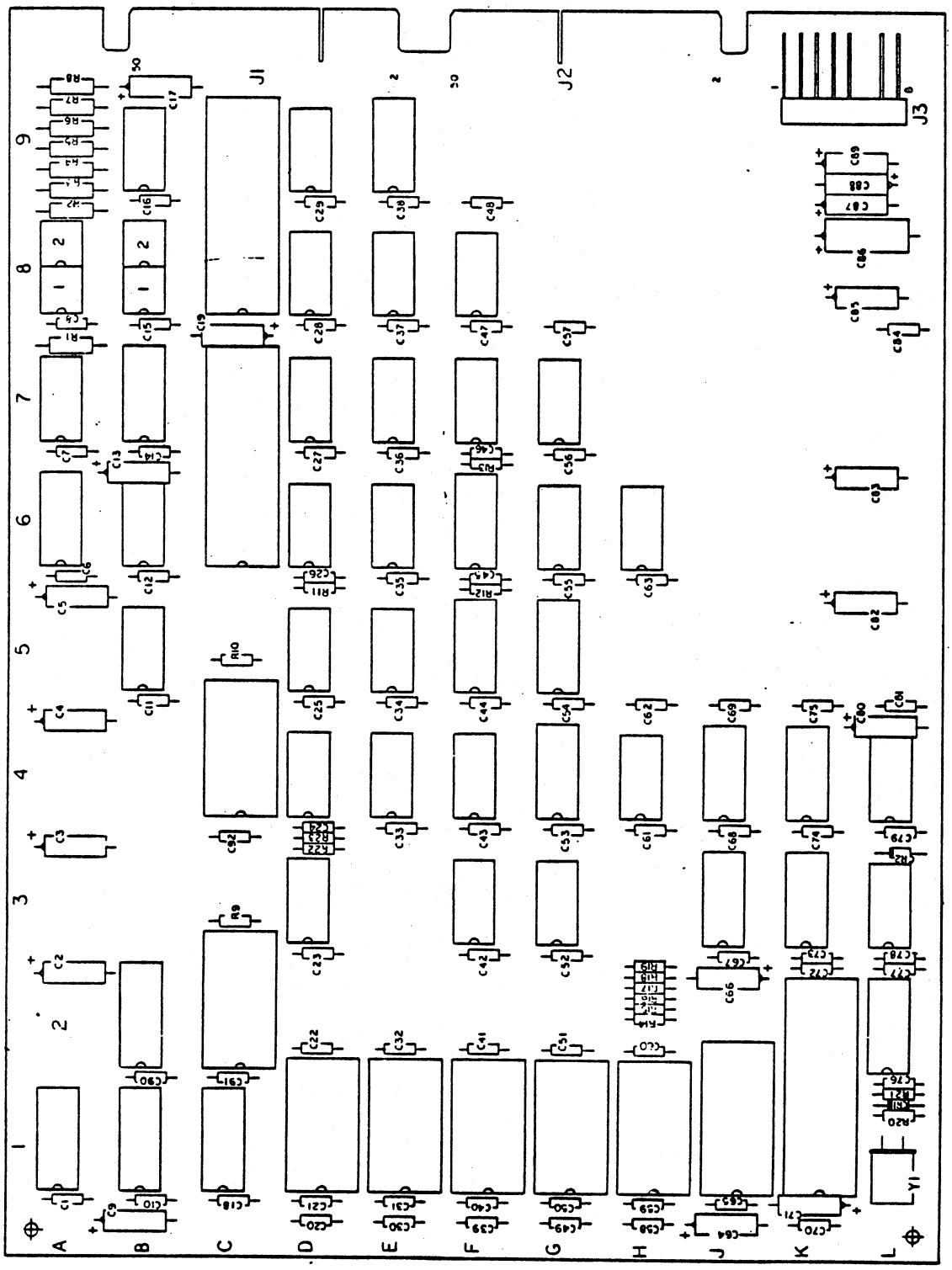


Figure 5-5. PWA Microprocessor No. 2 - (Sheet 2 of 11)

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	75896602-2	PWA Microprocessor No. 2	Used on 75897100-6
2	77834570-2	PWB Microprocessor No. 2	
5	17184200-8	I.C. 74193	
6	51761500-1	I.C. 74161	
7	15114700-6	I.C. 7432	
8	96744156-9	I.C. 7474	
9	15158300-2	I.C. 7438	
10	66299099-3	I.C. 7400	
11	66299100-9	I.C. 7410	
12	39389700-4	I.C. 7404	
13	88897000-1	I.C. 7408	
14	66299103-3	I.C. 7402	
15	36187300-3	I.C. 7420	
17	15148000-1	I.C. 74LS109	
18	15113000-2	I.C. 75452	
19	15138300-7	I.C. 8080A	
20	15140400-1	I.C. 8097	
21	15155400-3	I.C. 8212	
22	15153500-2	I.C. 8224	
23	15153400-5	I.C. 8228	
25	15153300-7	I.C. 8255	
26	15160200-0	I.C. 8257	
27	15106900-2	I.C. 9334	
28	66299110-8	I.C. 7442A	
29	15151600-2	I.C. 8111	
30	36186501-7	I.C. MC1489A	
31	95894500-8	Res Pac 220/330	
32	39465705-0	Crystal 18 MHz	
33	24500139-1	Res 1/2W 5% 100	
34	24500063-3	Res 1/4W 5% 1K	
35	24500071-6	Res 1/4W 5% 2.2K	
36	92496227-7	Cap 100V 20% .01 uF	
37	24504353-4	Cap 10V 20% 33 uF	
38	77830465-9	Socket 18 Pin	
39	94260301-0	Socket 16 Pin	
40	51858100-4	Socket 24 Pin	
41	51858101-2	Socket 28 Pin	
42	51858103-8	Socket 40 Pin	
46	15144900-6	I.C. 74LS00	
47	15129700-9	I.C. 7411	
48	77600006-9	Right Angle Header	
49	24504382-3	Cap 20V 20% 10 uF	
50	24504356-7	Cap 10V 20% 100 uF	
51	24500075-7	Res 1/4W 5% 3.3K	
52	24500087-2	Res 1/4W 5% 10K	
53	51736700-9	Diode IN914A	
54	24500059-1	Res 1/4W 5% 680	
55	75897051-1	PROM 1H	
56	75897060-2	PROM 1G	
57	75897071-9	PROM 1F	
58	75897080-0	PROM 1E	

Figure 5-5. PWA Microprocessor No. 2 - (Sheet 3 of 11)

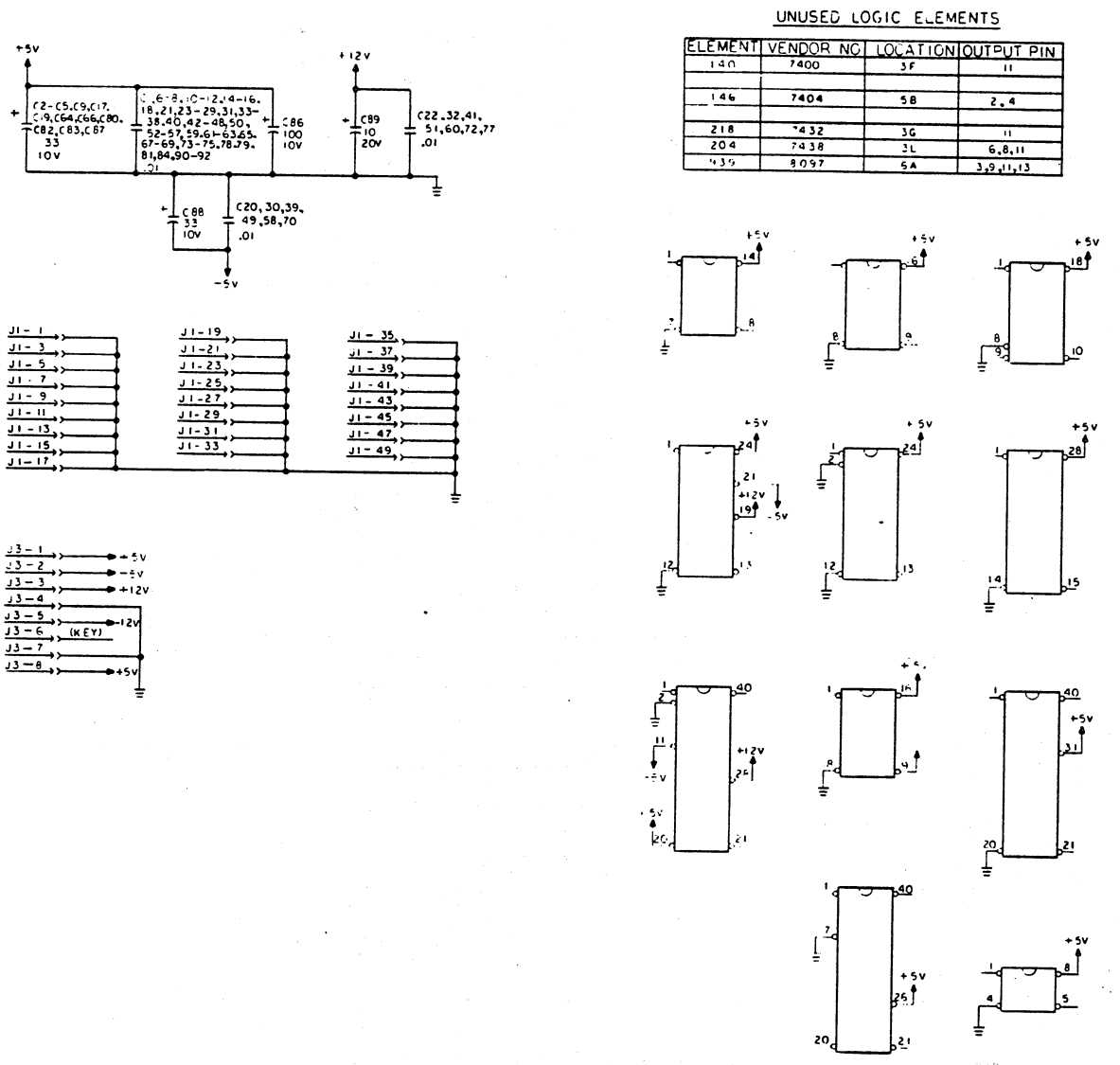


Figure 5-5. PWA Microprocessor No. 2 - (Sheet 4 of 11)

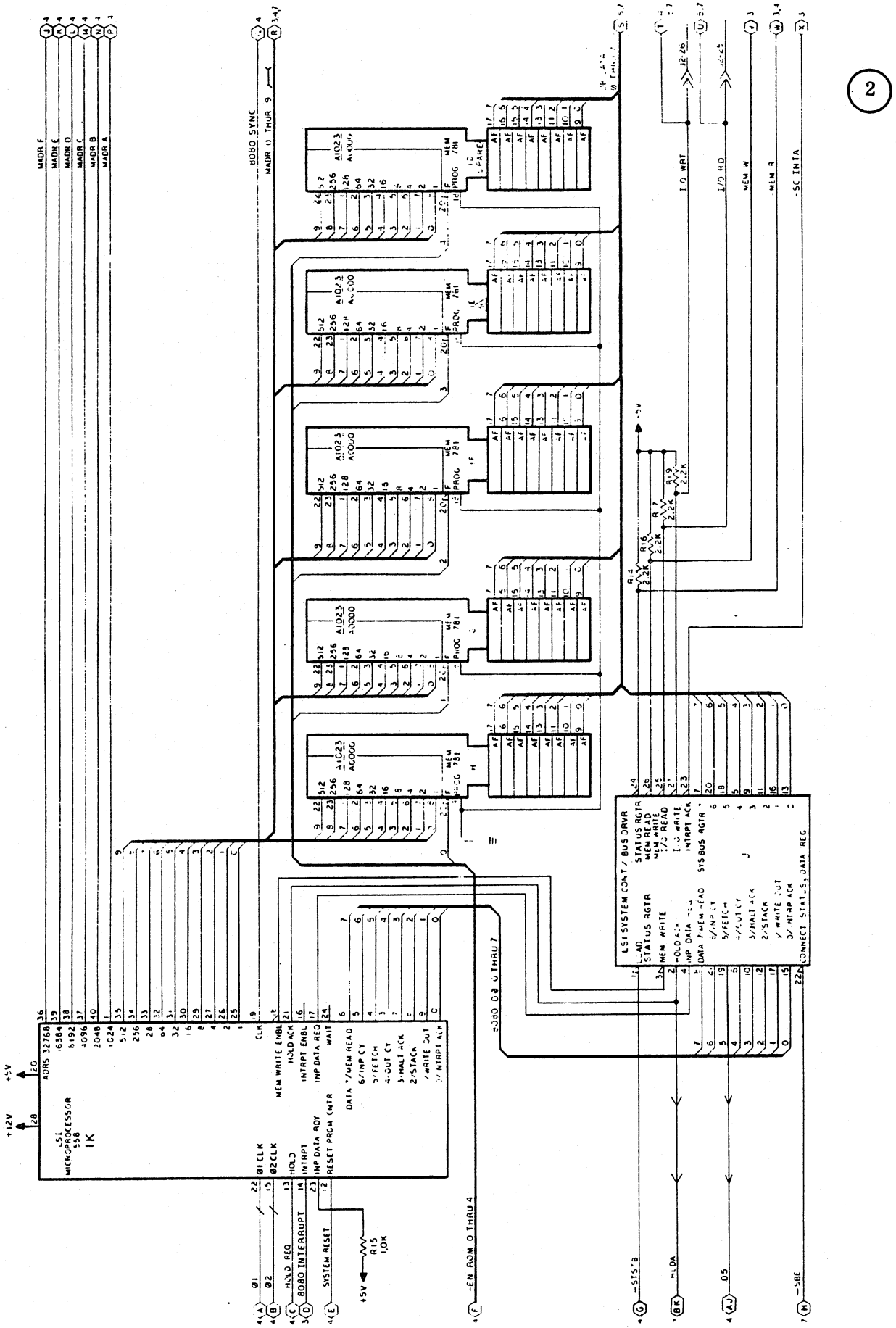


Figure 5-5. PWA Microprocessor No. 2 - (Sheet 5 of 11)

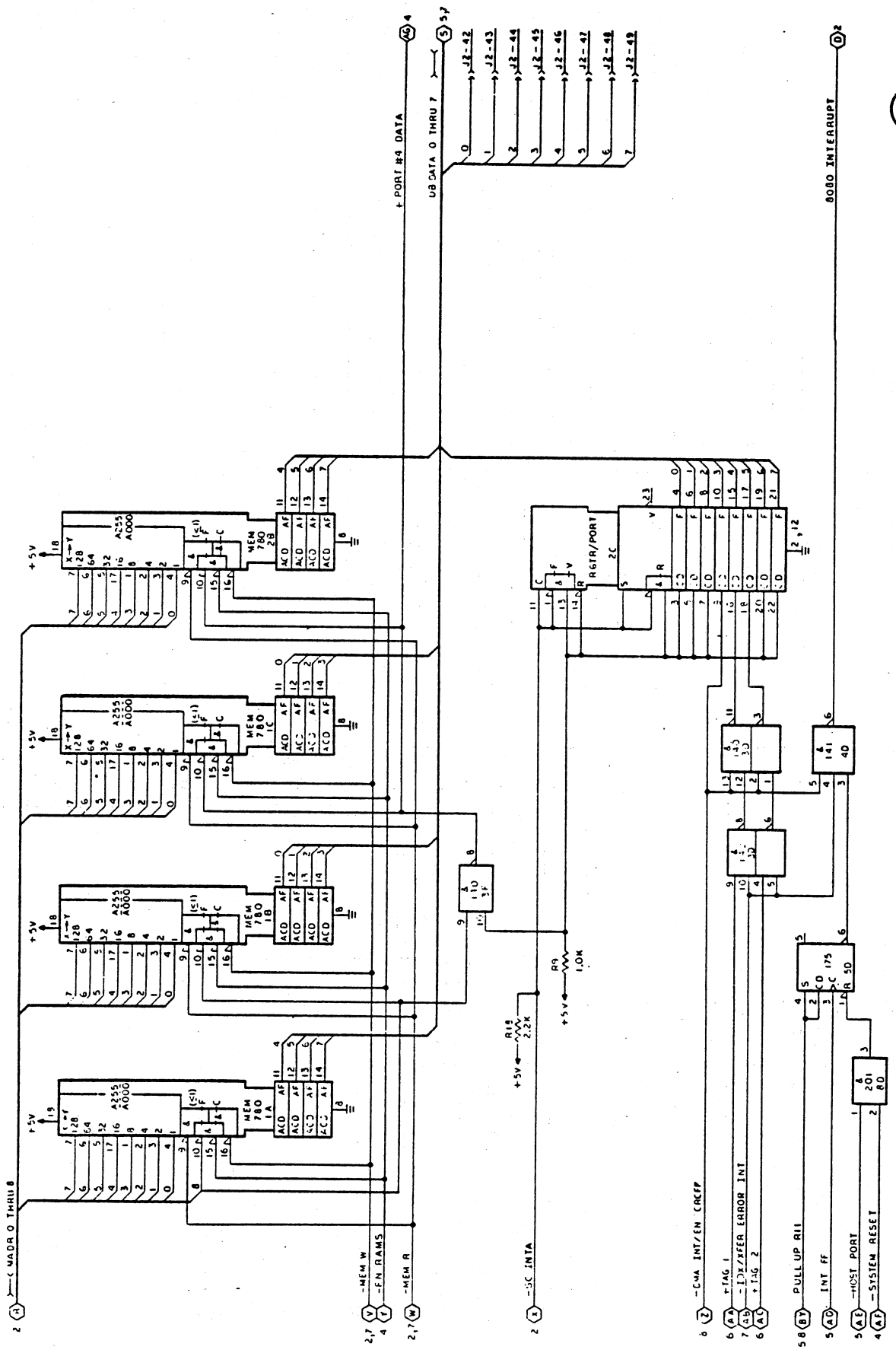


Figure 5-5. PWA Microprocessor No. 2 - (Sheet 6 of 11)

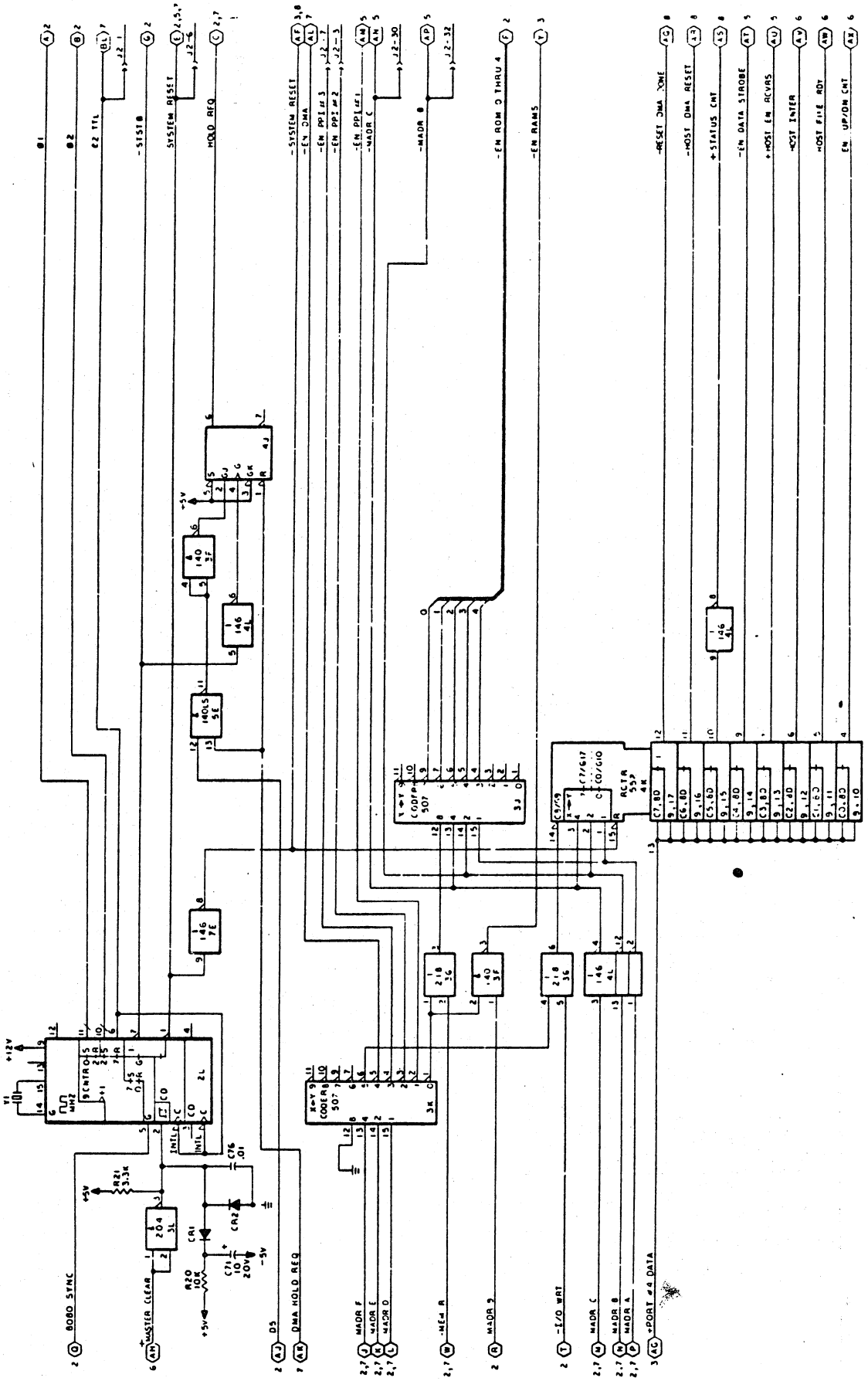


Figure 5-5. PWA Microprocessor No. 2 - (Sheet 7 of 11)

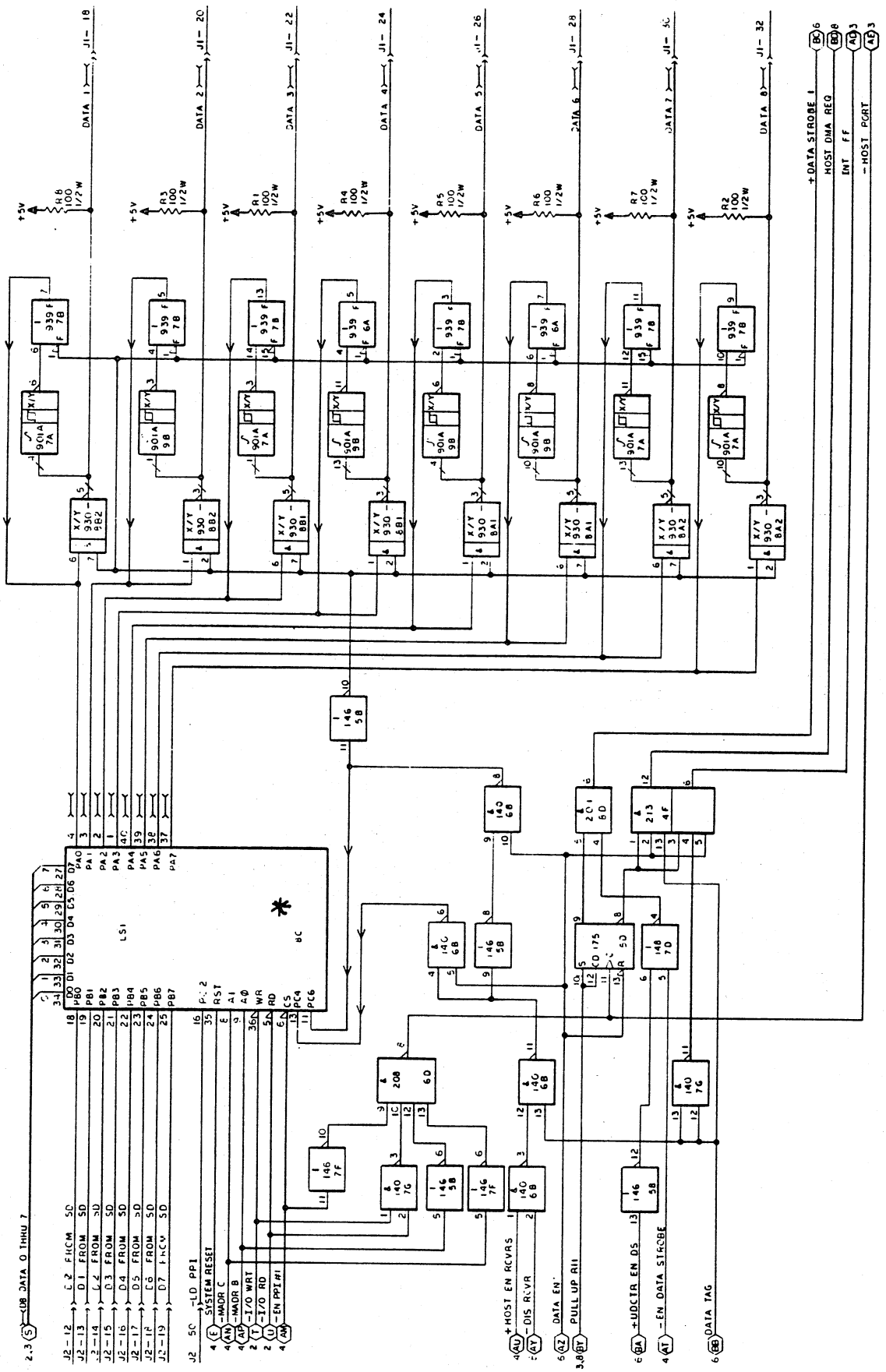


Figure 5-5. PWA Microprocessor No. 2 - (Sheet 8 of 11)

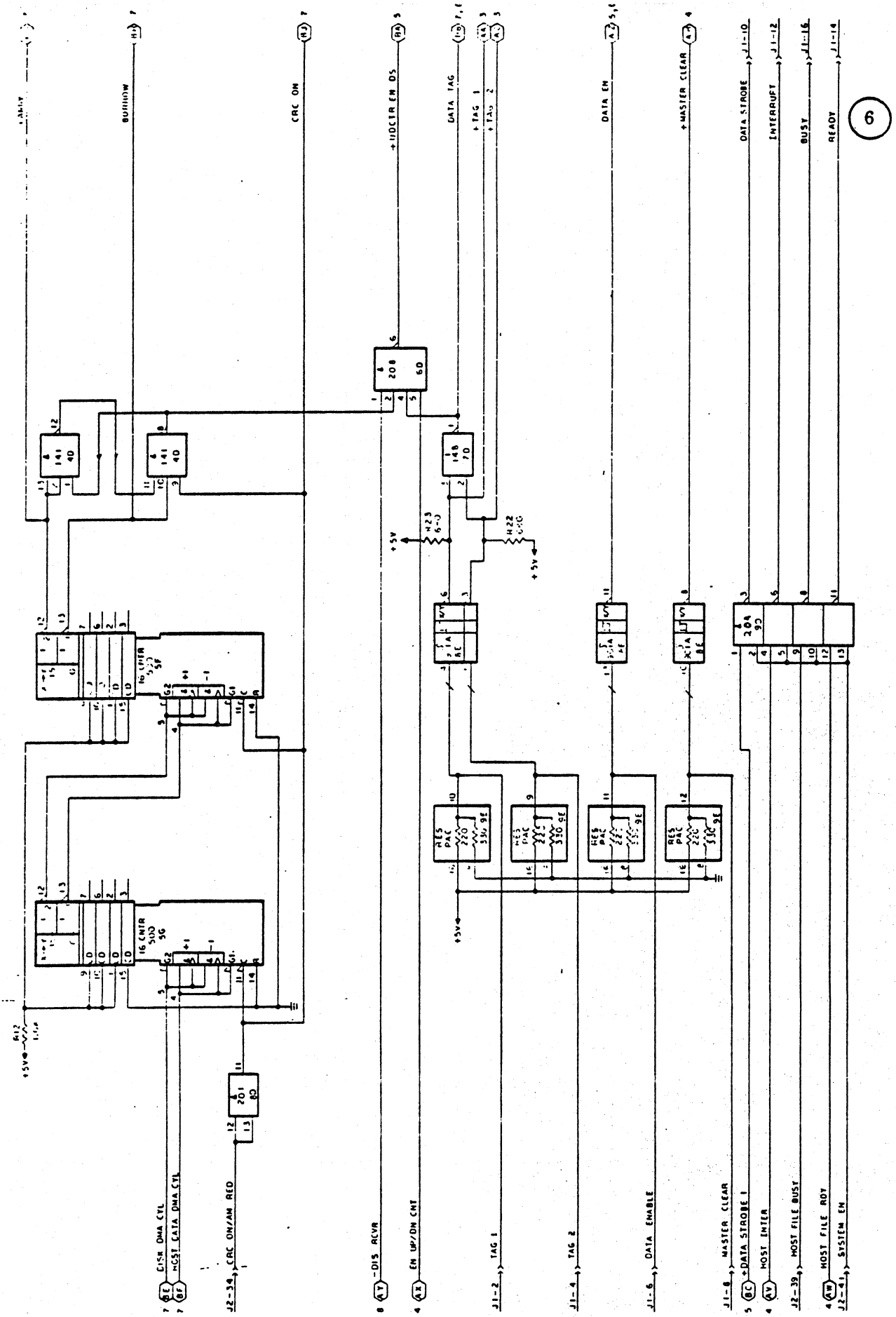


Figure 5-5. PWA Microprocessor No. 2 - (Sheet 9 of 11)

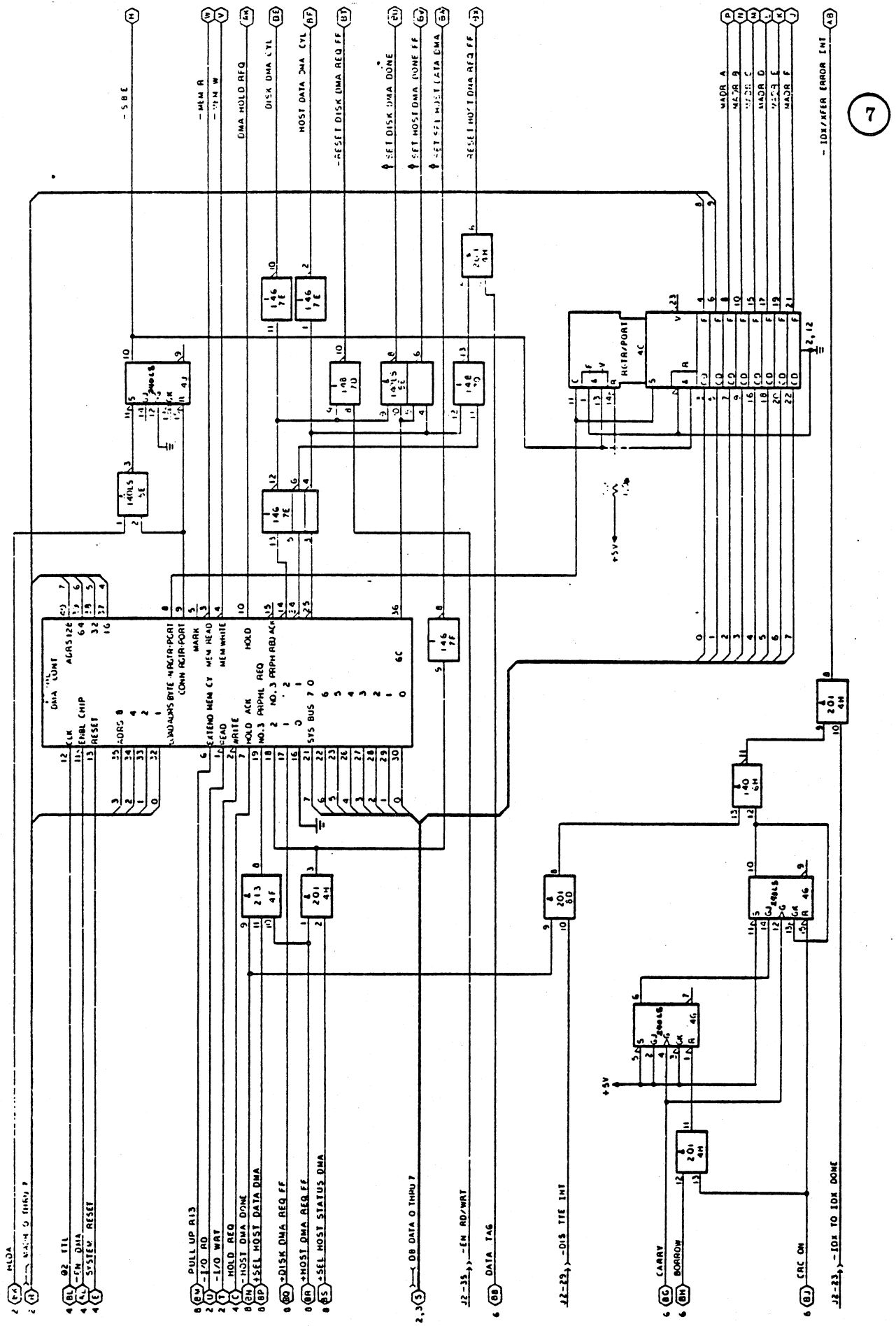


Figure 5-5. PWA Microprocessor No. 2 - (Sheet 10 of 11)

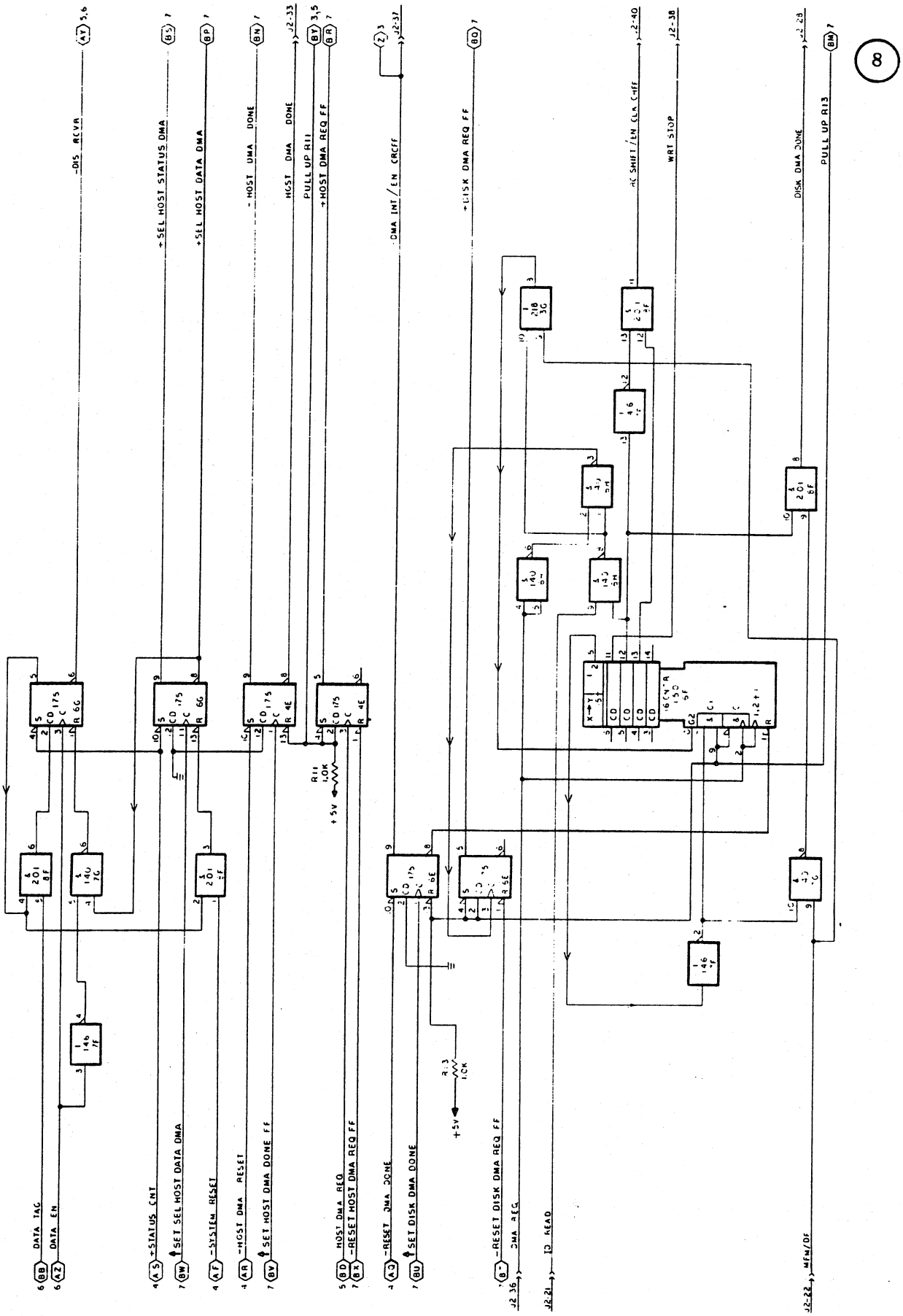
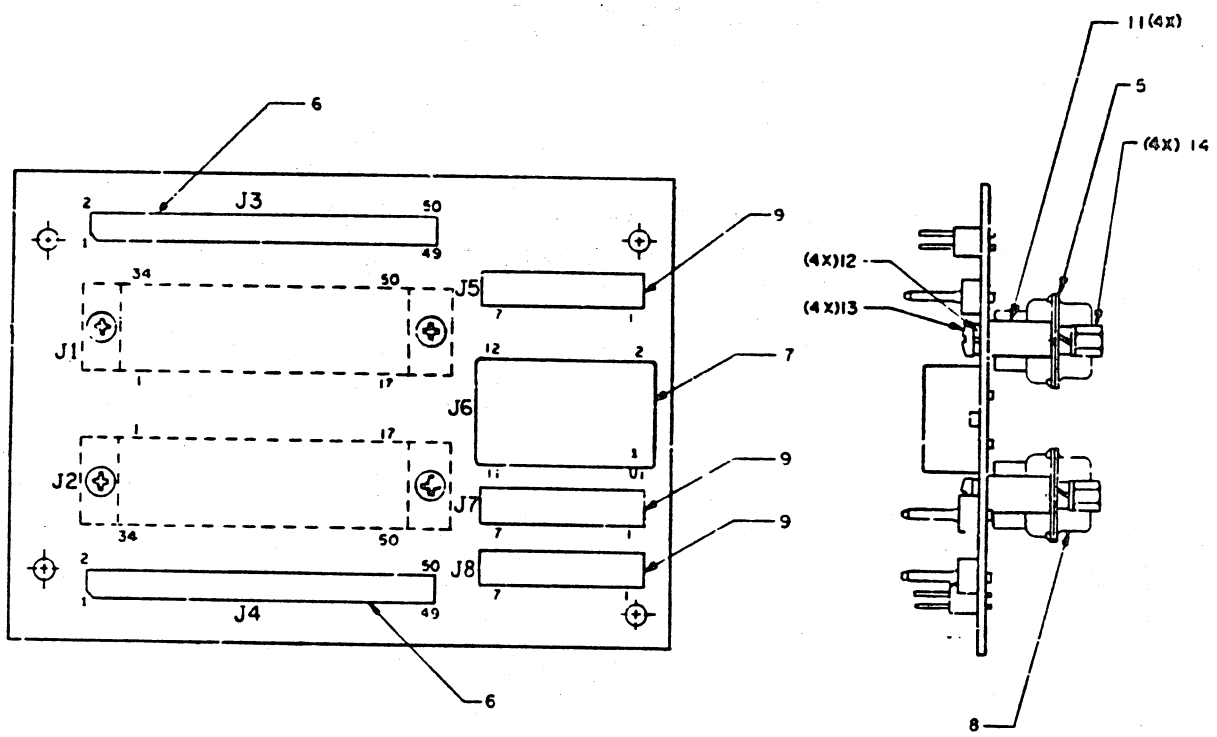


Figure 5-5. PWA Microprocessor No. 2 - (Sheet 11 of 11)



ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77834600-7	PWA I/O No. 1	Used on 77836060-2
2	77834620-5	PWB I/O No. 1	
5	83465801-5	Plug Connector	
6	83434524-1	Header, Amp	
7	95882803-0	Header, 12 Pin	
8	83465802-3	Recept 50 Pin	
9	77831965-7	Header	
11	83452411-8	Bushing, Standoff	
12	10125801-0	Spring Lock Washer	
13	10127102-1	Screw Pan Hd	
14	18252501-4	Scr Lock Assy	

Figure 5-6. PWA I/O No. 1 (Master) - (Sheet 1 of 2)

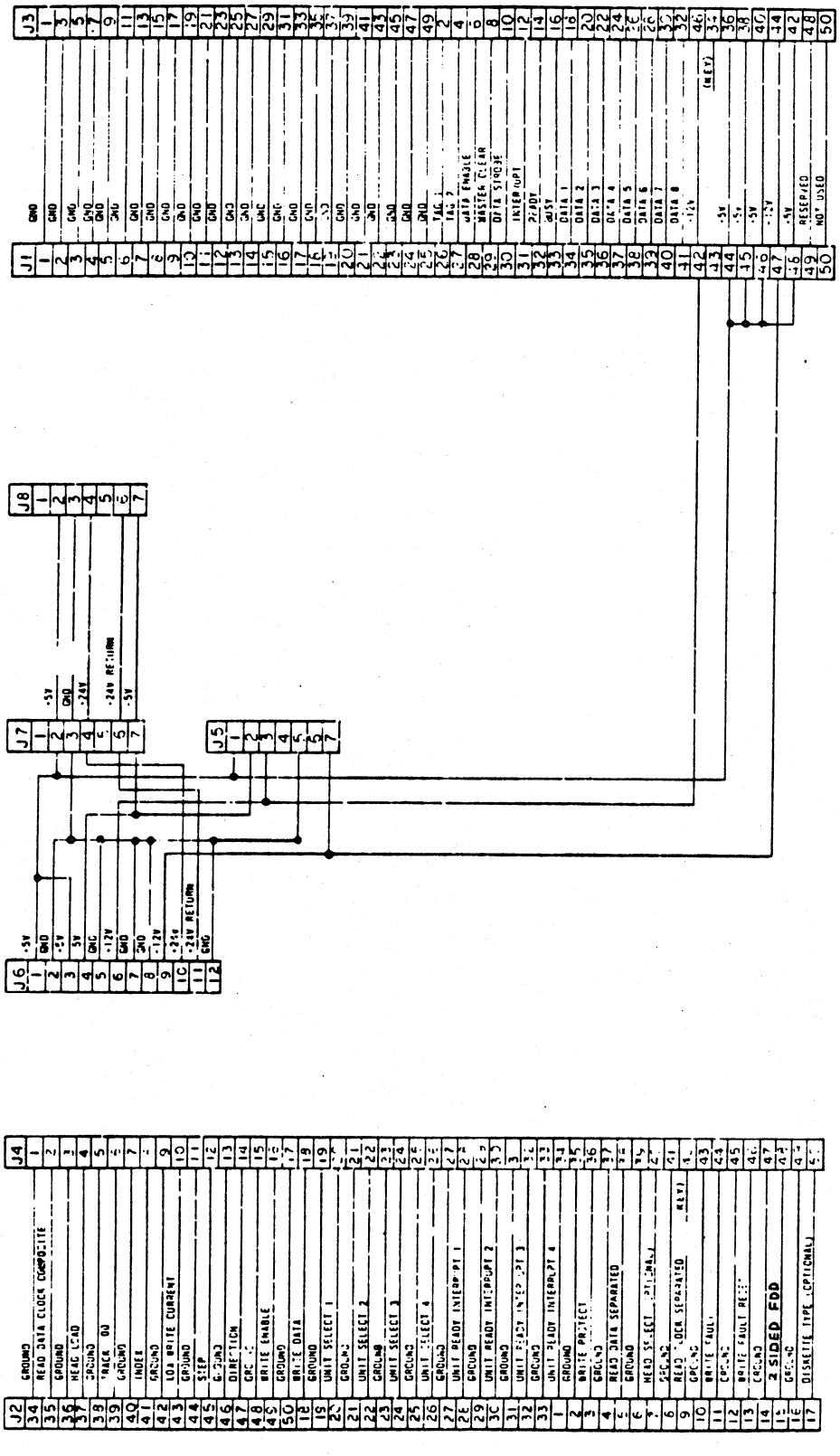
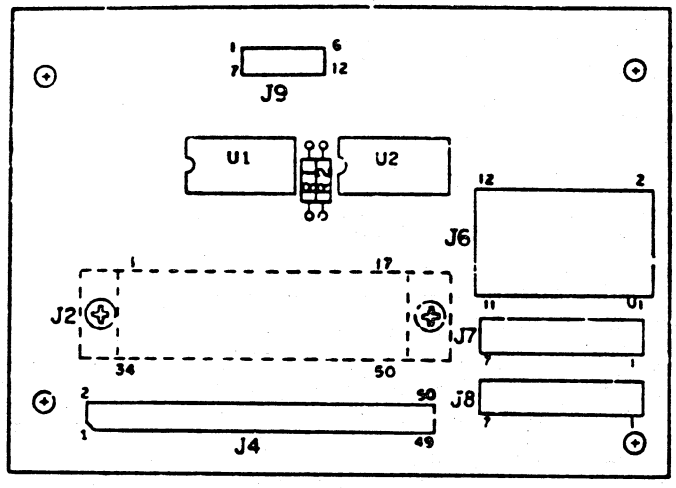
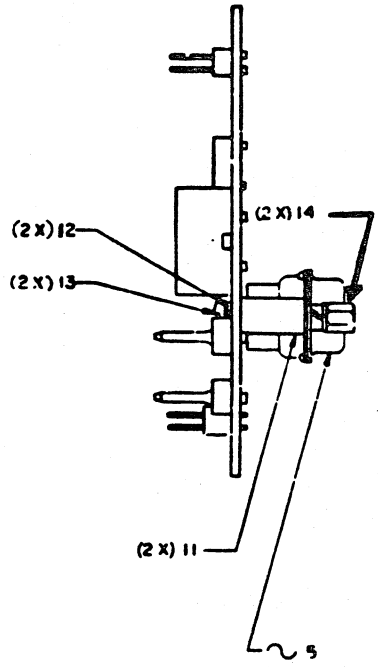


Figure 5-6. PWA I/O No. 1 (Master) - (Sheet 2 of 2)





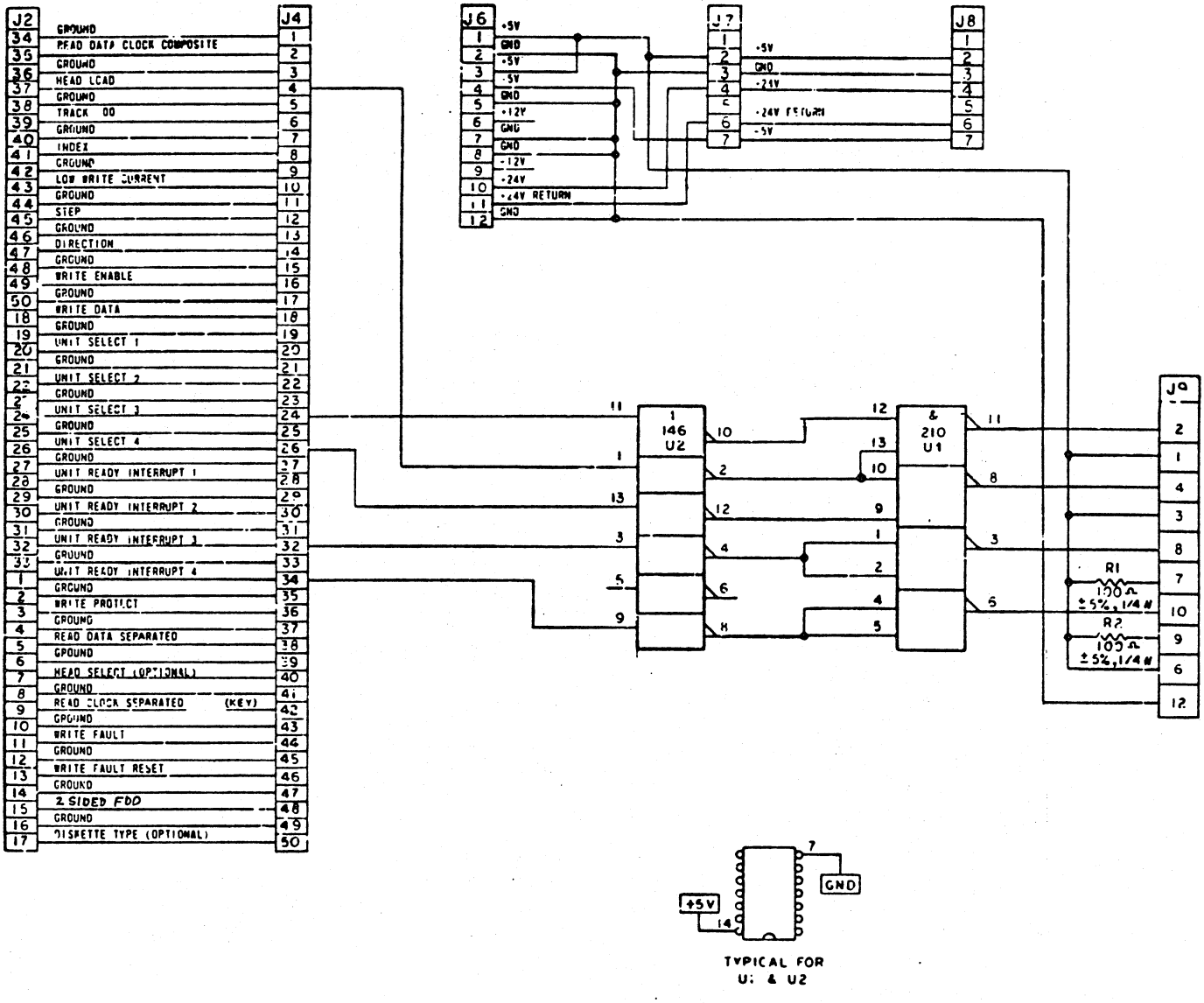
CONN	ITEM NO.
J2	5
J4	6
J6	7
J7	9
J8	9
J9	10

IC	ITEM NO.
U1	15
U2	16

RES	ITEM NO.
R1	17
R2	17

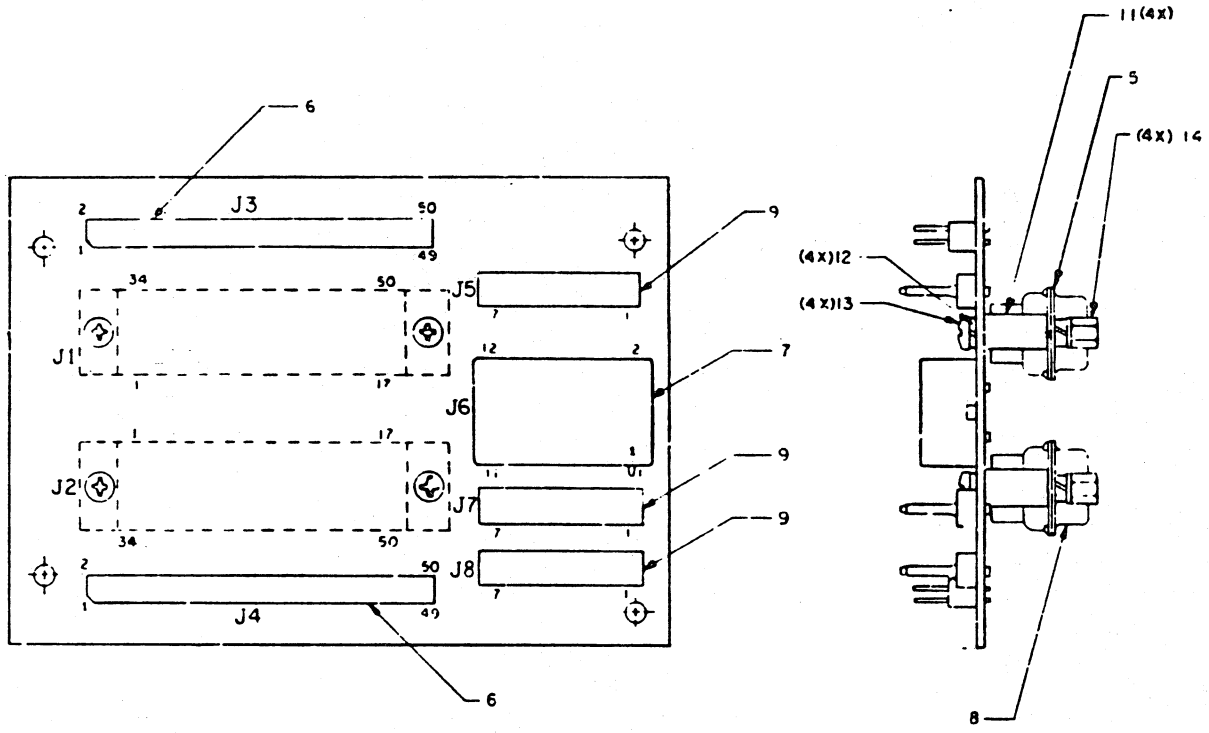
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77834450-7	PWA I/O No. 2	Used on 77836061-0
2	77834470-5	PWB I/O No. 2	
5	83465802-3	Recept 50 Pin	
6	83434524-1	Header, Amp	
7	95882803-0	Header, 12 Pin	
9	77831965-7	Header	
10	83434505-0	Header, 12 Pin	
11	83452411-8	Bushing, Standoff	
12	10125801-0	Spring Lock Washer	
13	10127102-1	Screw Pan Hd	
14	18252501-4	Scr Lock Assy	
15	15107000-0	I. C. 7437	
16	39389700-4	I. C. 7404	
16	36187100-7	I. C. 7404	
17	24500039-3	Res 1/4W 5% 100	

Figure 5-7. PWA I/O No. 2 (Slave) - (Sheet 1 of 2)



TYPICAL FOR
U1 & U2

Figure 5-7. PWA I/O No. 2 (Slave) - (Sheet 2 of 2)



ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	75895750-0	PWA I/O No. 3	Used on 77614550-0
2	75895770-7	PWB I/O No. 3	
5	83465801-5	Plug Connector	
6	83434524-1	Header, Amp	
7	95882803-0	Header, 12 Pin	
8	83465802-3	Recept 50 Pin	
9	77831965-7	Header	
11	83452411-8	Bushing, Standoff	
12	10125801-0	Spring Lock Washer	
13	10127102-1	Screw Pan Hd	
14	18252501-4	Scr Lock Assy	

Figure 5-7a. PWA I/O No. 3 (Master) - (Sheet 1 of 2)

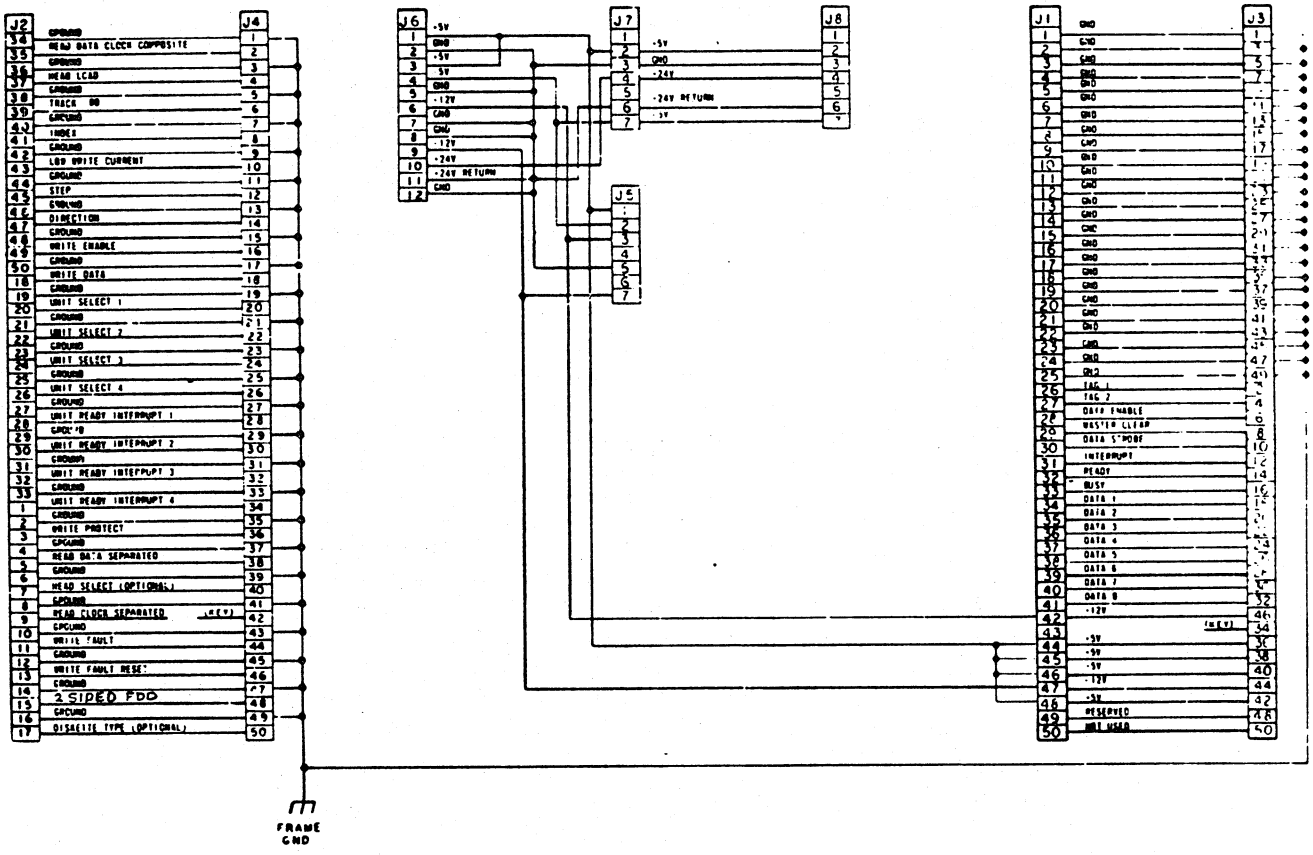
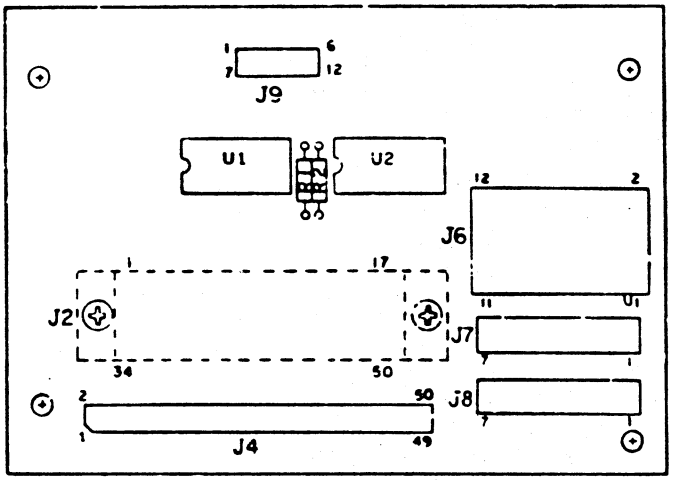
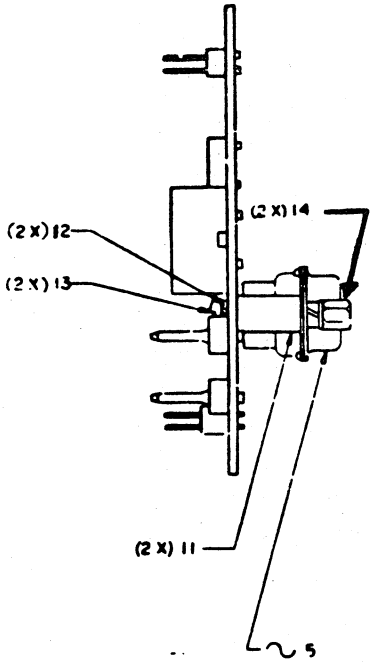


Figure 5-7a. PWA I/O No. 3 (Master) - (Sheet 2 of 2)





CONN	ITEM NO.
J2	5
J4	6
J6	7
J7	9
J8	9
J9	10

IC	ITEM NO.
U1	15
U2	16

RES	ITEM NO.
R1	17
R2	17

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	75895800-3	PWA I/O No. 4	Used on 77614551-8
2	75895820-1	PWB I/O No. 4	
5	83465802-3	Recept 50 Pin	
6	83434524-1	Header, Amp	
7	95882803-0	Header, 12 Pin	
9	77831965-7	Header	
10	83434505-0	Header, 12 Pin	
11	83452411-8	Bushing, Standoff	
12	10125801-0	Spring Lock Washer	
13	10127102-1	Screw Pan Hd	
14	18252501-4	Scr Lock Assy	
15	15107000-0	I. C. 7437	
16	39389700-4	I. C. 7404	
16	36187100-7	I. C. 7404	
17	24500039-3	Res 1/4W 5% 100	

Figure 5-7b. PWA I/O No.4 (Slave) - (Sheet 1 of 2)

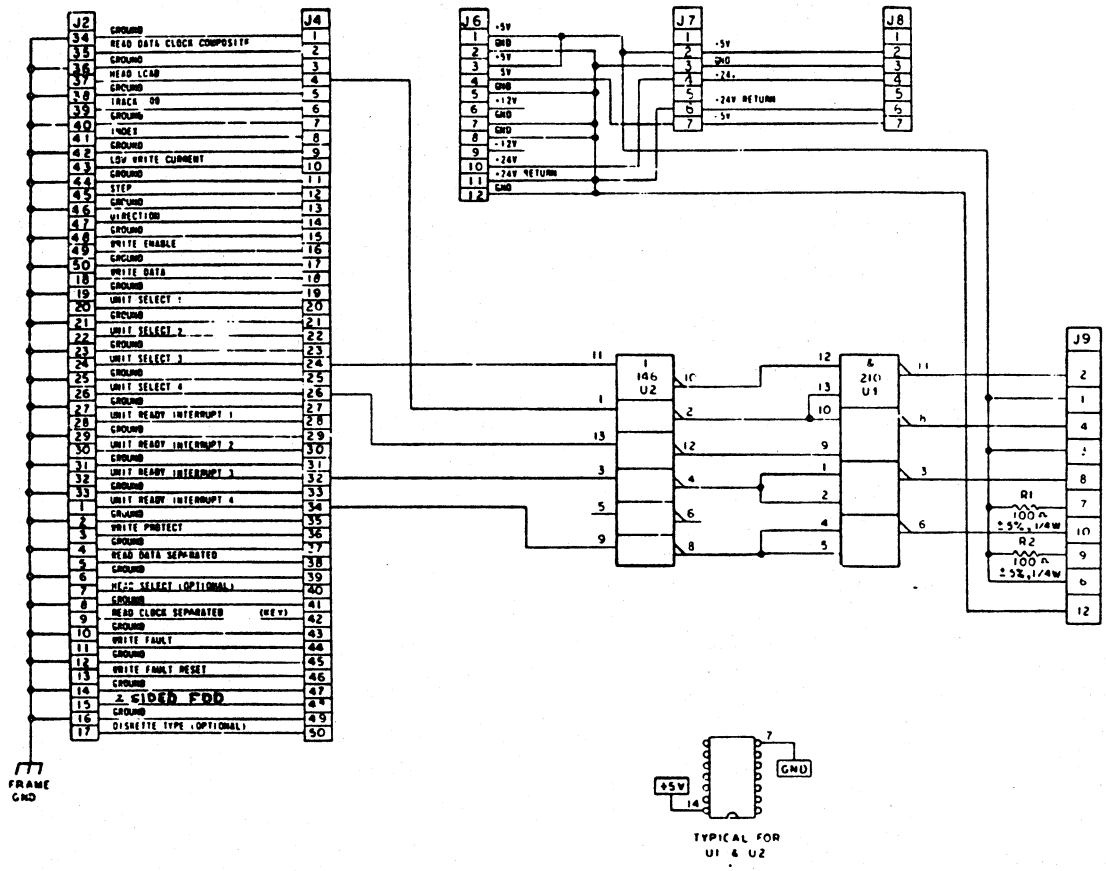
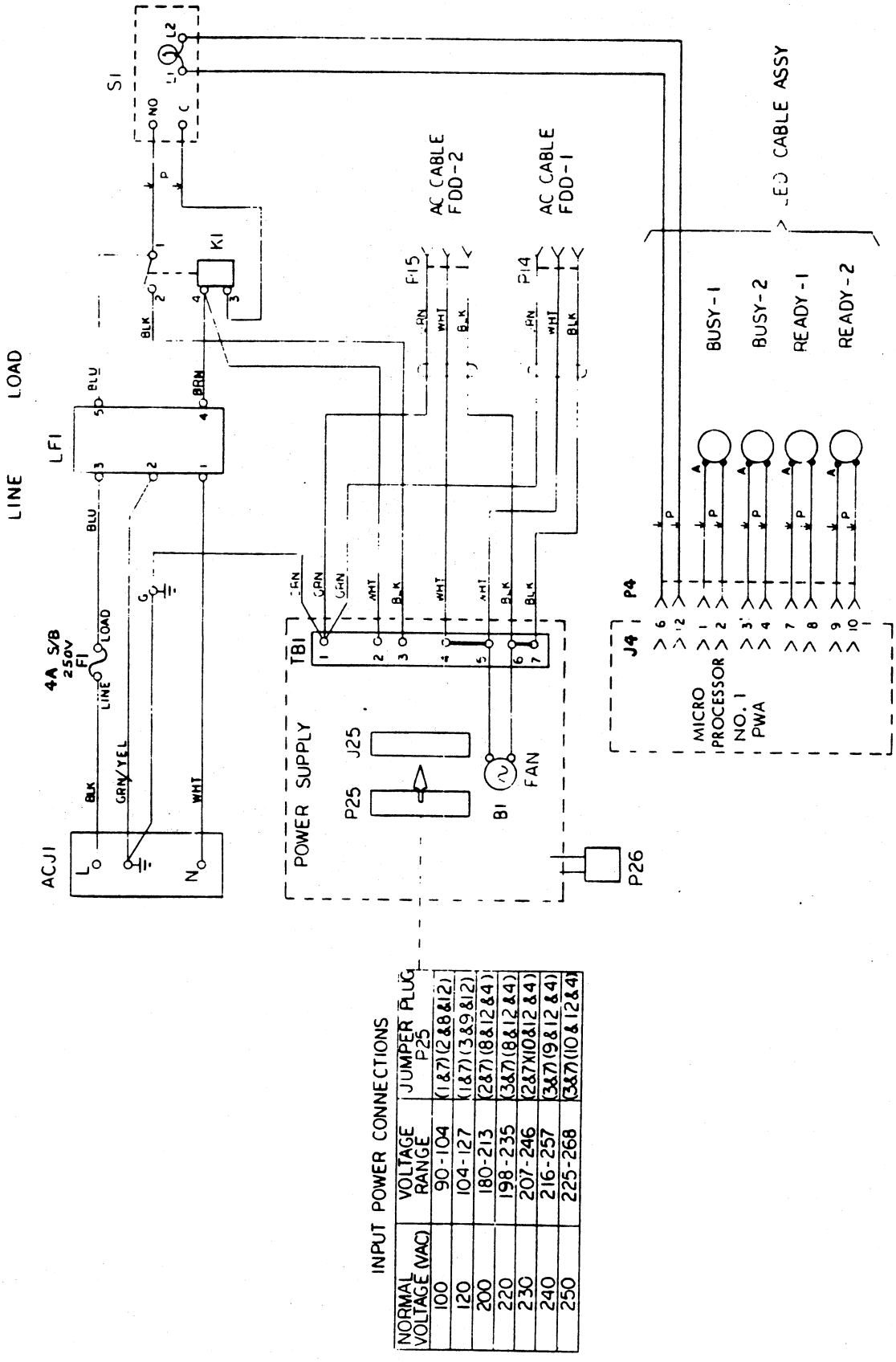


Figure 5-7b. PWA I/O No.4 (Slave) - (Sheet 2 of 2)



INPUT POWER CONNECTIONS

NORMAL VOLTAGE (VAC)	VOLTAGE RANGE	JUMPER PLUG P25
100	90-104	(1&7)(2&8&12)
120	104-127	(1&7)(3&9&12)
200	180-213	(2&7)(8&12&4)
220	198-235	(3&7)(8&12&4)
230	207-246	(2&7)(10&12&4)
240	216-257	(3&7)(9&12&4)
250	225-268	(3&7)(10&12&4)

Figure 5-8. FDDS AC Power Interconnect Schematic

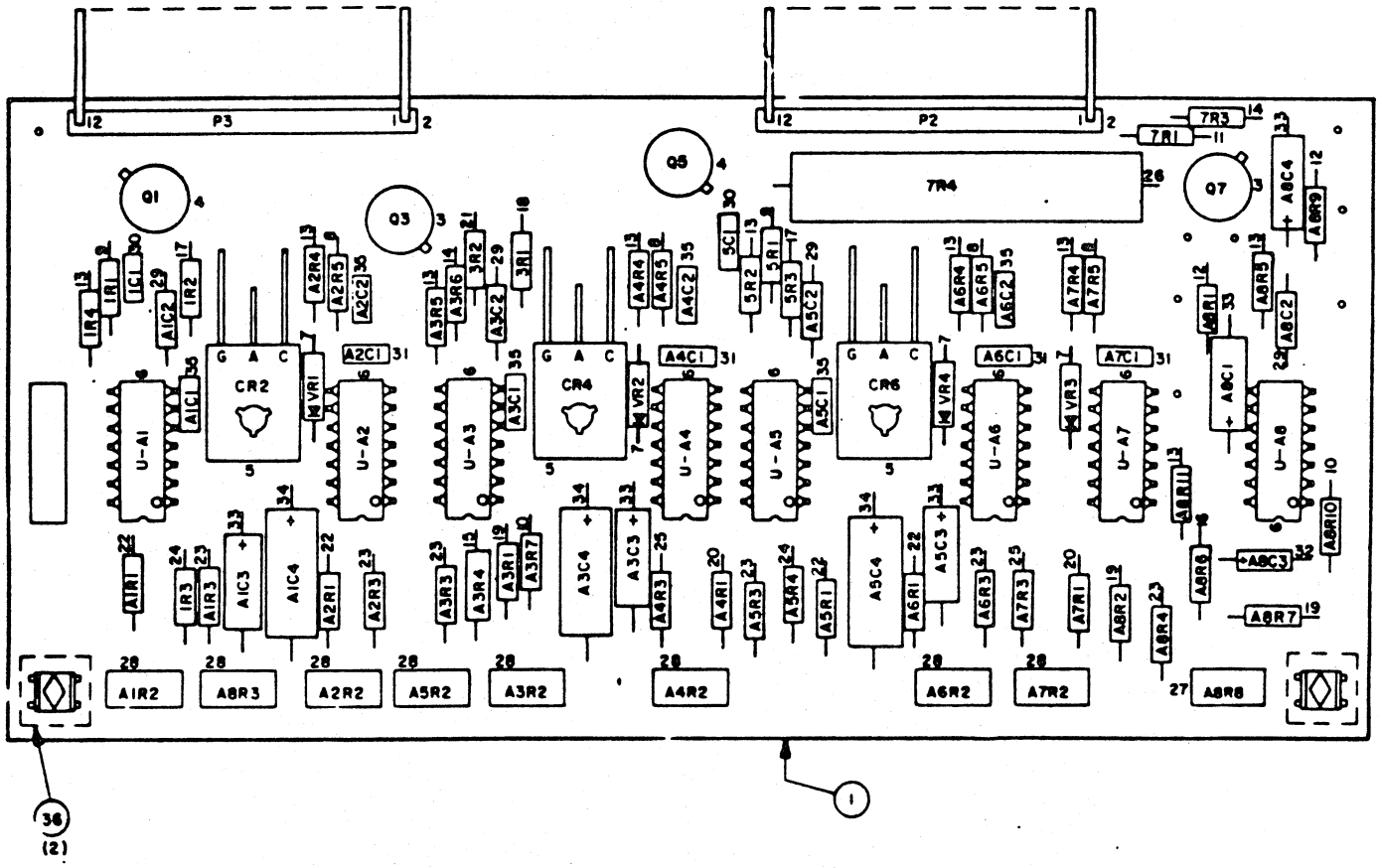


Figure 5-9. Type 6VZN PWA (Used on P/N 76835500 Power Supply) (Sheet 1 of 4)

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	76845400-1	Type 6VZN Comp Assy	Used on 76835500 Pwr Sply
1	76845300-3	Type 6VZN P-W Board	
2	94388401-5	Header-.045 Sq. Pin Right Ang.	
3	50210810-3	Tstr, SNPN, 60V NN3568, To 5	
4	95688601-4	Transistor, Silicon Pwr PNP	
5	94825900-7	Rectifier, Silicon Controlled	
6	51718400-8	I.C. Voltage Reg 40V, Max	
7	50240109-4	Diode, Silicon 6.8V 5 Ohm	
8	92512153-5	Resistor 1/4W 100 ohms	
9	92512156-8	Resistor 1/4W 270 ohms	
10	92512157-6	Resistor 1/4W 470 ohms	
11	92512162-6	Resistor 1/4W 4.7K ohms	
12	92512240-0	Resistor 1/4W 10 ohms	
13	92512248-3	Resistor 1/4W 68 ohms	
14	92512260-8	Resistor 1/4W 8.2K ohms	
15	92512809-2	Res 1/2W 150 ohm	
16	94360160-9	Res 42.2 ohms	
17	94360192-2	Res 90.9 ohms	
18	94360204-5	Res 110 ohms	
19	94360232-6	Res 215 ohms	
20	94360268-0	Res 511 ohms	
21	94360292-0	Res 909 ohms	
22	94360308-4	Res 1210 ohms	
23	94360324-1	Res 1780 ohms	
24	94360328-2	Res 1960 ohms	
25	94360368-8	Res 5110 ohms	
26	95594106-7	Resistor, Fixed 10W 10 ohms	
27	95597802-8	Pot., Trim 0.5 Watt 500 ohms	
28	95597803-6	Pot., Trim 0.5 Watt 1K ohms	
29	92496365-5	Cap Non-Electro 3300 pF	
30	95593001-1	Capacitor, Disk 1000V 220 pF	
31	95593006-0	Capacitor, Disk 1000V 470 pF	
32	92427027-5	Cap Electro 1 uF 35V	
33	92427039-0	Cap Electro 6.8 uF 35V	
34	92427136-6	Cap Electro 47 uF 20VDC	
35	51001119-0	Cap Non-Electro .01 uF 25V	
36	95533003-0	Nut, Push-In Nylon	

Figure 5-9. Type 6VZN PWA (Used on P/N 76835500 Power Supply) (Sheet 2 of 4)

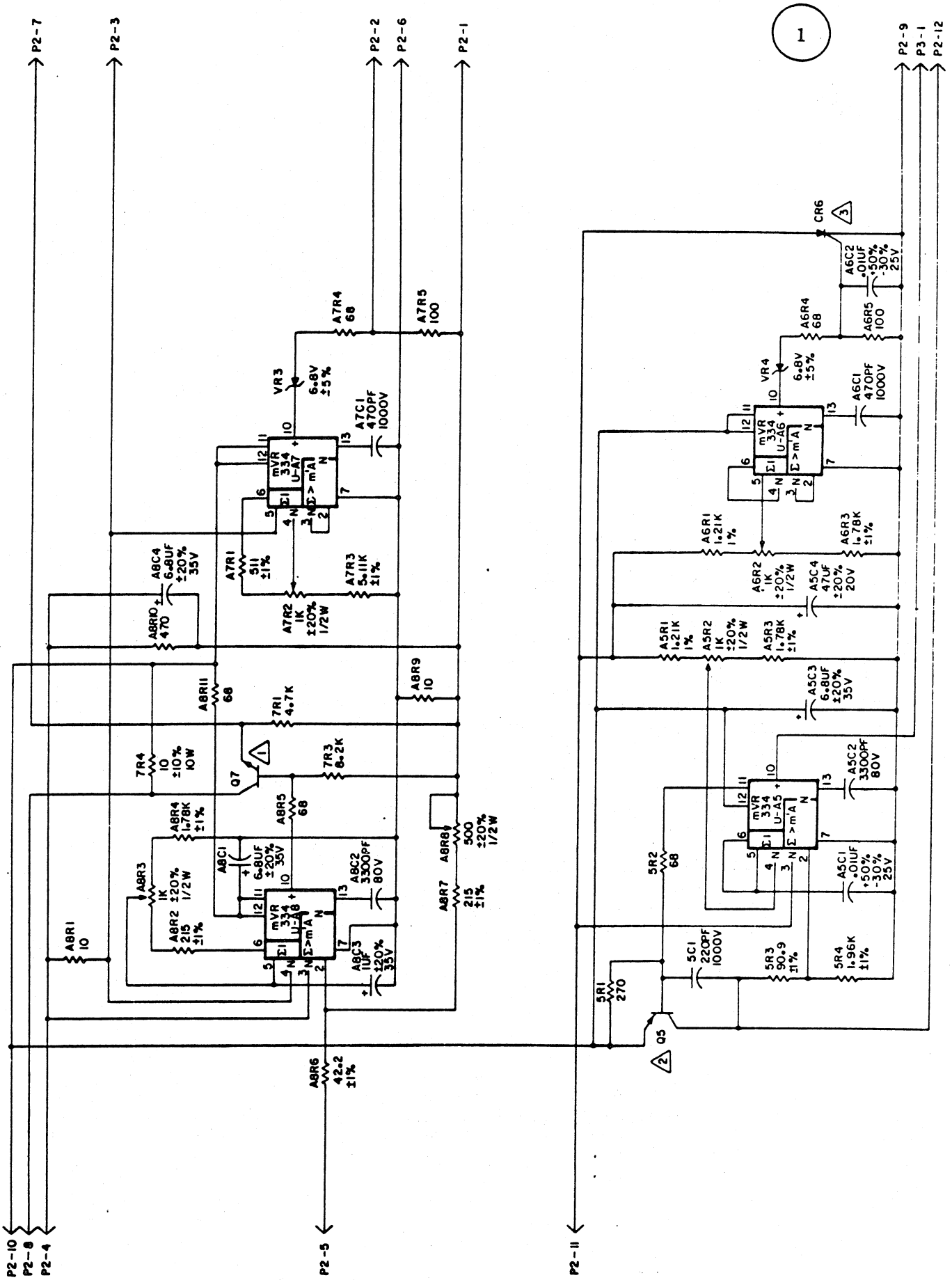


Figure 5-9. Type 6VZN PWA (Used on P/N 76835500 Power Supply) (Sheet 3 of 4)

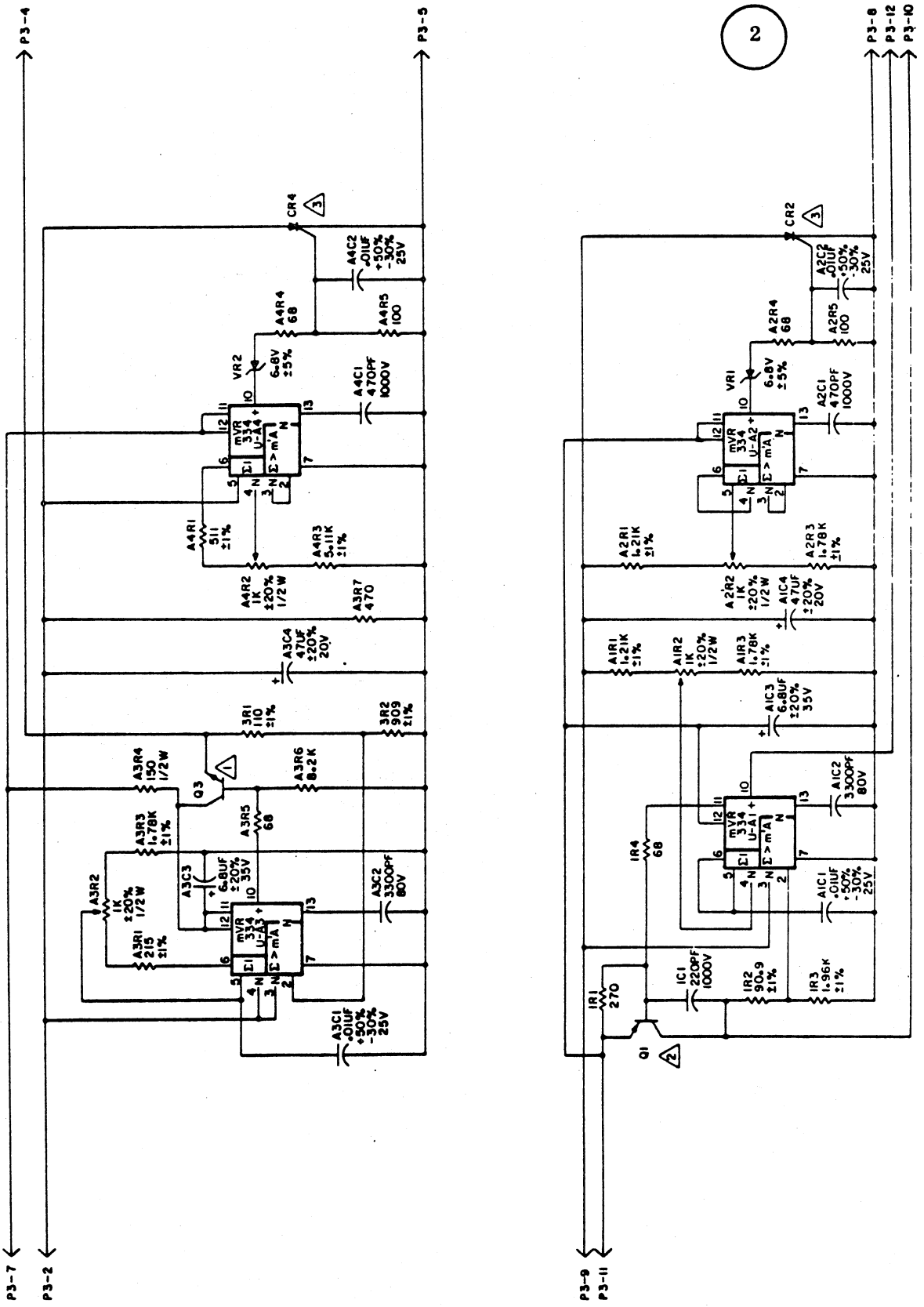


Figure 5-9. Type 6VZN PWA (Used on P/N 76835500 Power Supply) (Sheet 4 of 4)

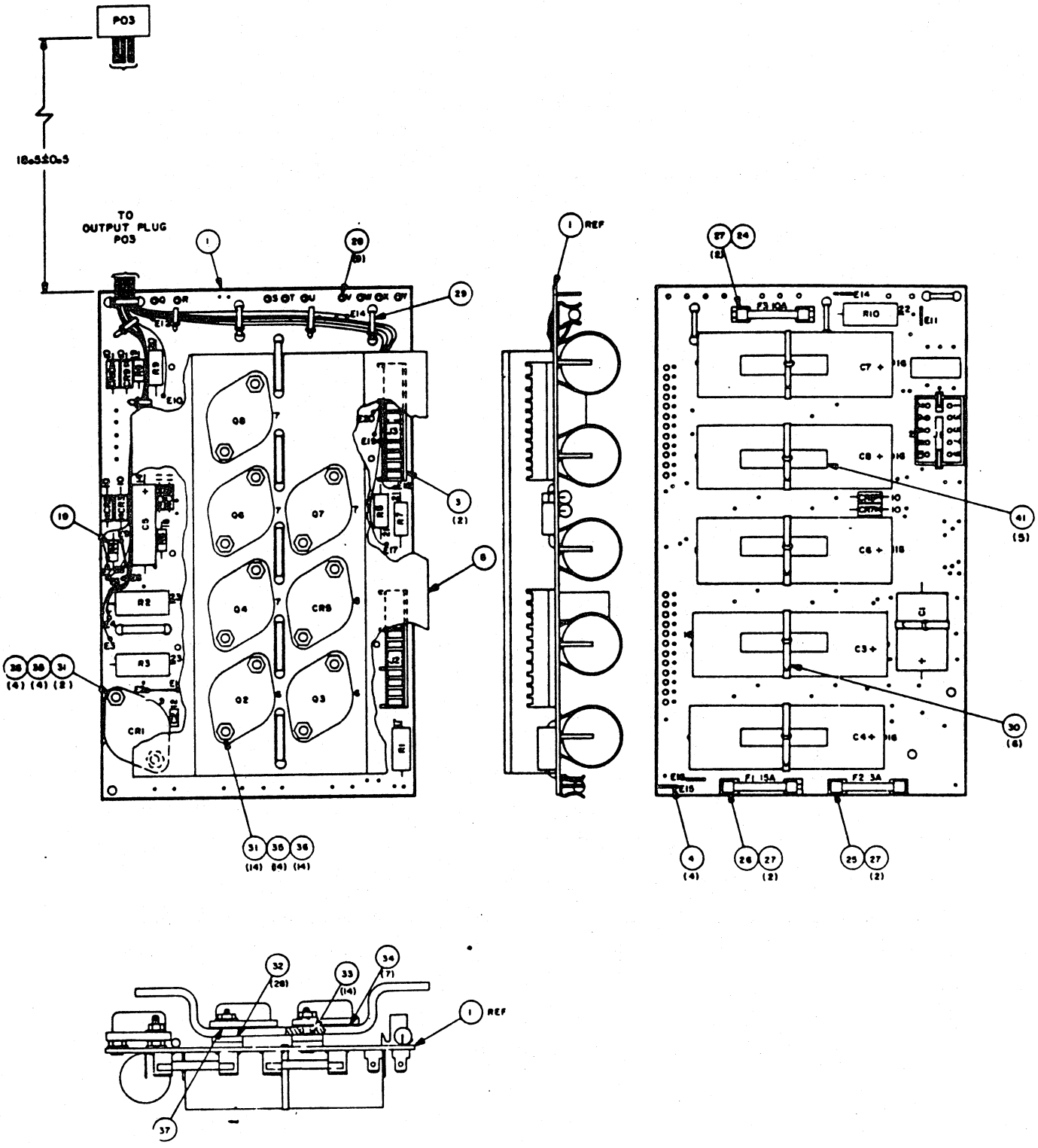


Figure 5-10. Type 6VYN PWA (Used on P/N 76835500 Power Supply) (Sheet 1 of 4)

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	76845000-9	Type 6VYN Comp. Assy FDDS	Used on 76835000 Power Supply
1	76844900-1	Type 6VYN Board Blank	
2	95882802-2	Pin Header Assy (Dbl Row)	
3	94388807-3	Connector-Bottom Entry, PC Bd	
4	95524700-2	Terminal .250 Quick Connect	
5	76847700-2	Heatsink-PC Board	
6	94791000-6	Tstr Sil NPN 150W 40V 2N3771	
7	95658800-8	Tstr Sil NPN 115 W 60 V2N3055	
8	95601100-1	Rectifier Package Com. Cathode	
9	95597600-6	Rect Sil Cont. 12 Amp 100V	
10	95588200-6	Rect Sil 3 Amp 100V	
11	93935000-5	Rectifier, Silicon	
12	51001119-0	Cap Non-Electro .01 uF 25V	
13	92427150-5	Cap Electro 850 uF 10V	
14	92427153-9	Cap, Electro 470 uF 16V	
15	95577003-7	Cap Alum Elect 15 VDC 14000 mF	
16	94497401-9	Capacitor, 7500 mF	
17	92512571-8	Resistor 2W 220 ohms	
18	92512825-8	Res 1/2W 1K ohm	
19	92512837-3	Res 1/2W 3.9K ohms	
20	94389112-7	Resistor 2W Flameproof	
21	94389120-0	Resistor 2W Flameproof	
22	95596519-9	Res., Fixed W/Wd 5W 510 ohms	
23	95596546-2	Res., Fixed W/Wd 5W .08 ohms	
24	93418239-5	Fuse 1/4X/ 1/4Glass	
25	95647603-0	Fuse, Quick-Acting 3 Amp	
26	95647609-7	Fuse, Quick-Acting 15 Amp	
27	95588400-2	Clip, Fuse	
28	92498021-2	Terminal, Swager	
29	94277400-1	Cable Tie Strap 1/15-5/8 Dia	
30	94277411-8	Strap, Cable Tie	
31	95683511-0	Stud, Press	
32	95797300-1	Washer, Phenolic	
33	95644207-3	Bushing, Insul	
34	94783900-7	Mica Washer	
35	95510030-0	Nut, Hex Brass 6-32	
36	95524400-9	Washer Lock Bronze 6	

Figure 5-10. Type 6VYN PWA (Used on P/N 76835500 Power Supply) (Sheet 2 of 4)

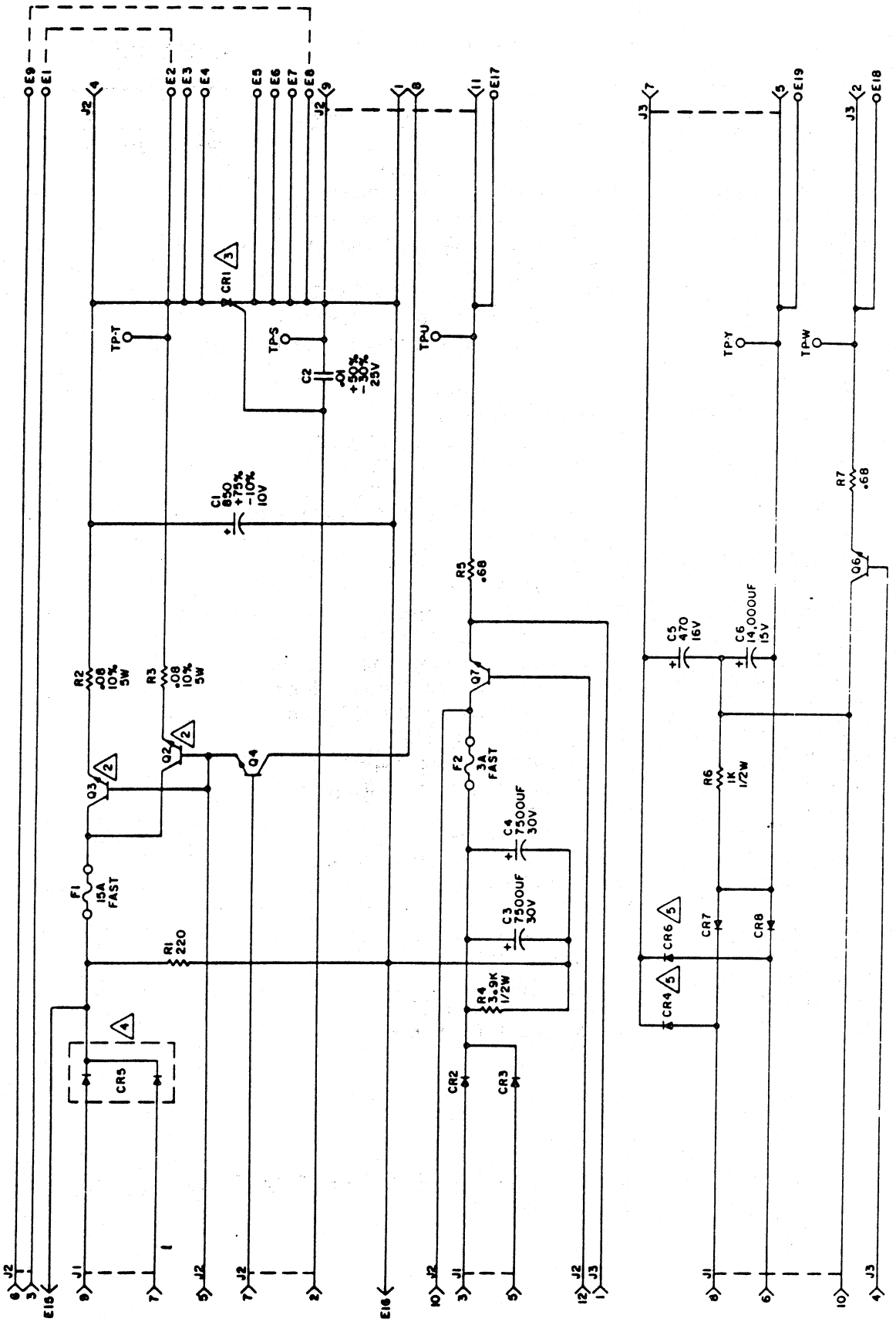


Figure 5-10. Type 6VYN PWA (Used on P/N 76835500 Power Supply) (Sheet 3 of 4)

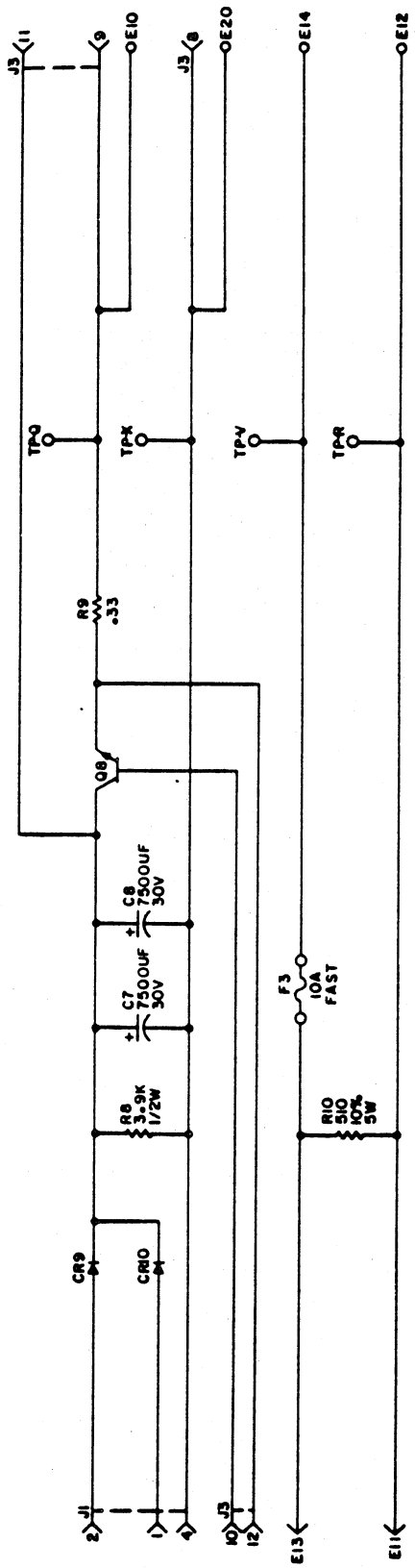


Figure 5-10. Type 6VYN PWA (Used on P/N 76835500 Power Supply) (Sheet 4 of 4)

INPUT POWER CONNECTIONS

NORMAL VOLTAGE (VAC)	VOLTAGE RANGE	JUMPER PLUG P25
100	90-104	(1&7)(2&8&12)
120	104-127	(1&7)(3&9&12)
200	180-213	(2&7)(8&12&4)
220	198-235	(3&7)(8&12&4)
230	207-246	(2&7)(10&12&4)
240	216-257	(3&7)(9&12&4)
250	225-268	(3&7)(10&12&4)

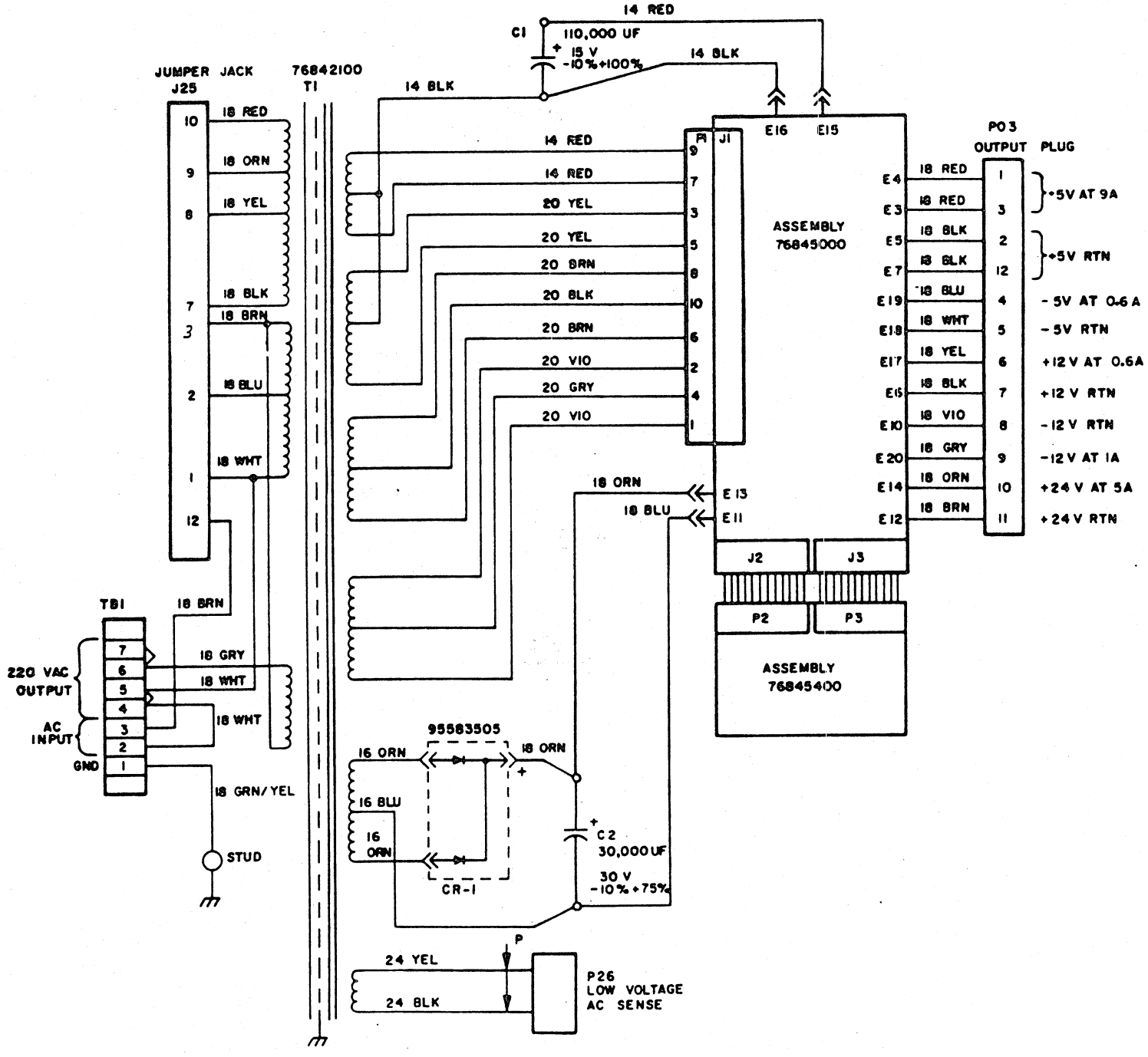


Figure 5-11. Power Supply Schematic/Wiring

VI
MAINTENANCE

6.1 INTRODUCTION

There are no instructions necessary to maintain the Flexible Disk Drive Subsystem other than that which is provided in the FDD Maintenance Manual which should accompany the FDDS. No preventative maintenance is needed to that part of the FDDS which excludes the FDD units. See Section 6 for test points and adjustments in the event that adjustments should become necessary. Adjustments should rarely be needed, however.

VII MAINTENANCE AIDS

7.1 GENERAL

7.2 PRINTED CIRCUIT BOARD LOCATION

Location of the Printed Circuit Boards is shown in Figure 7-1.

7.3 TEST POINTS AND ADJUSTMENTS

Test point and adjustment control locations and adjustment procedures are given in the following paragraphs. See Figures 7-2 through 7-7 also.

7.3.1 POWER SUPPLY TEST POINTS AND ADJUSTMENTS

The following power supply voltage readings apply to the FDDS fully connected, non-operating (idle) mode.

1. +5.1V +1%
2. -5.0V ±1%
3. +12.0V ±1%
4. -12.0V ±1%
5. +24V not adjustable

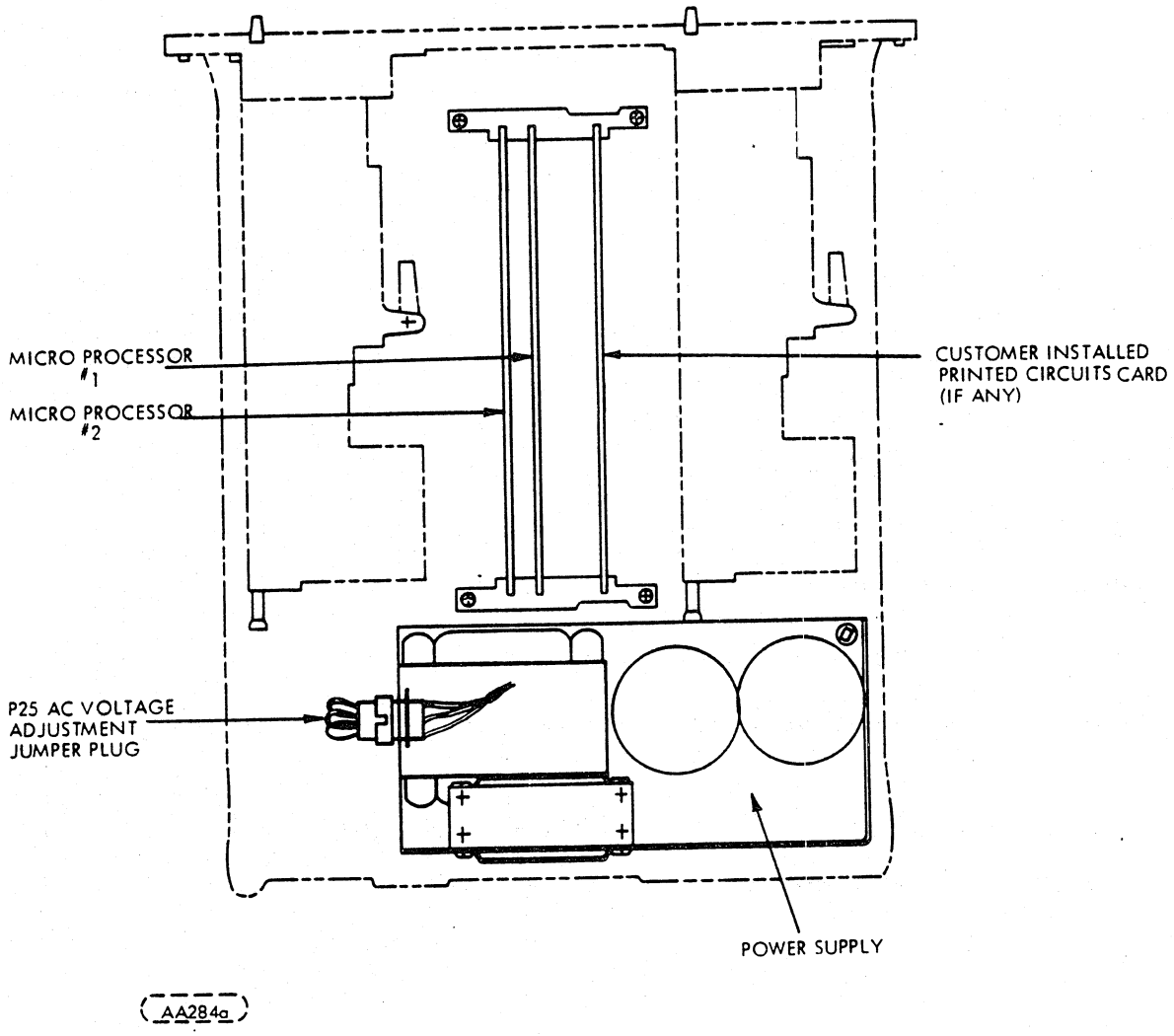


Figure 7-1. Printed Circuit Board Locations

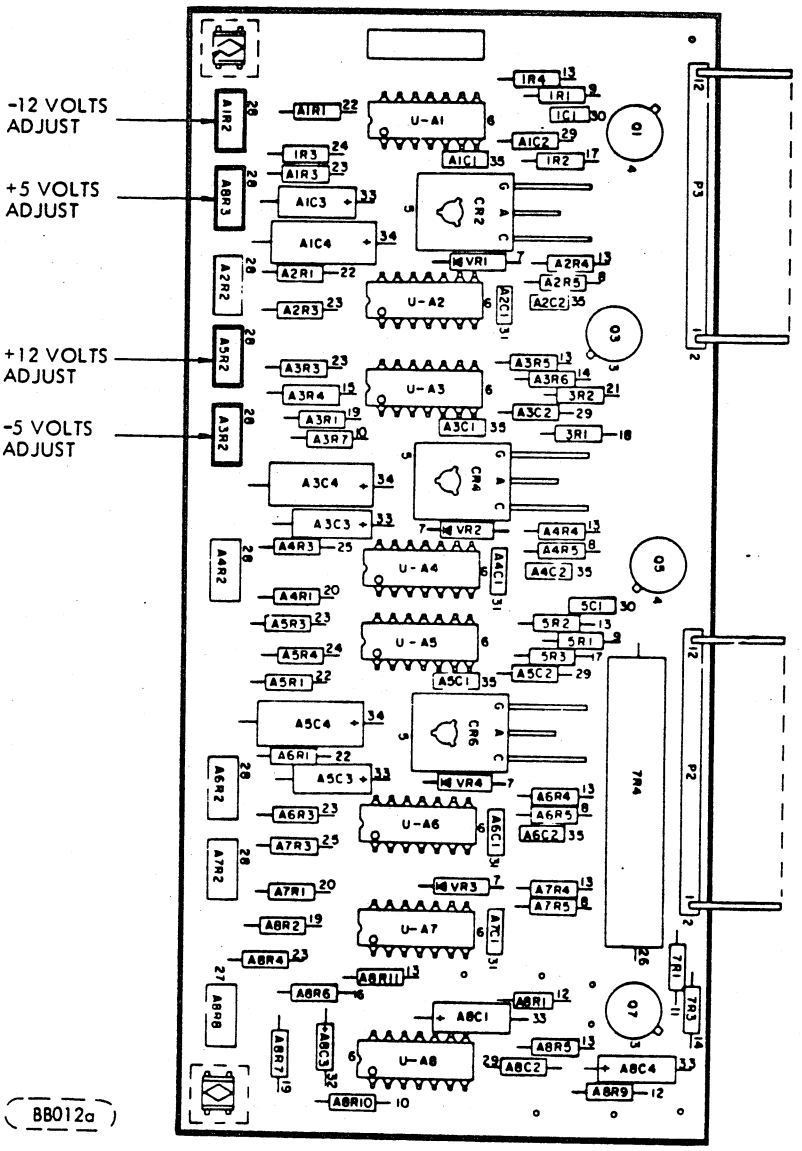


Figure 7-2. Voltage Adjustment Locations for Power Supply

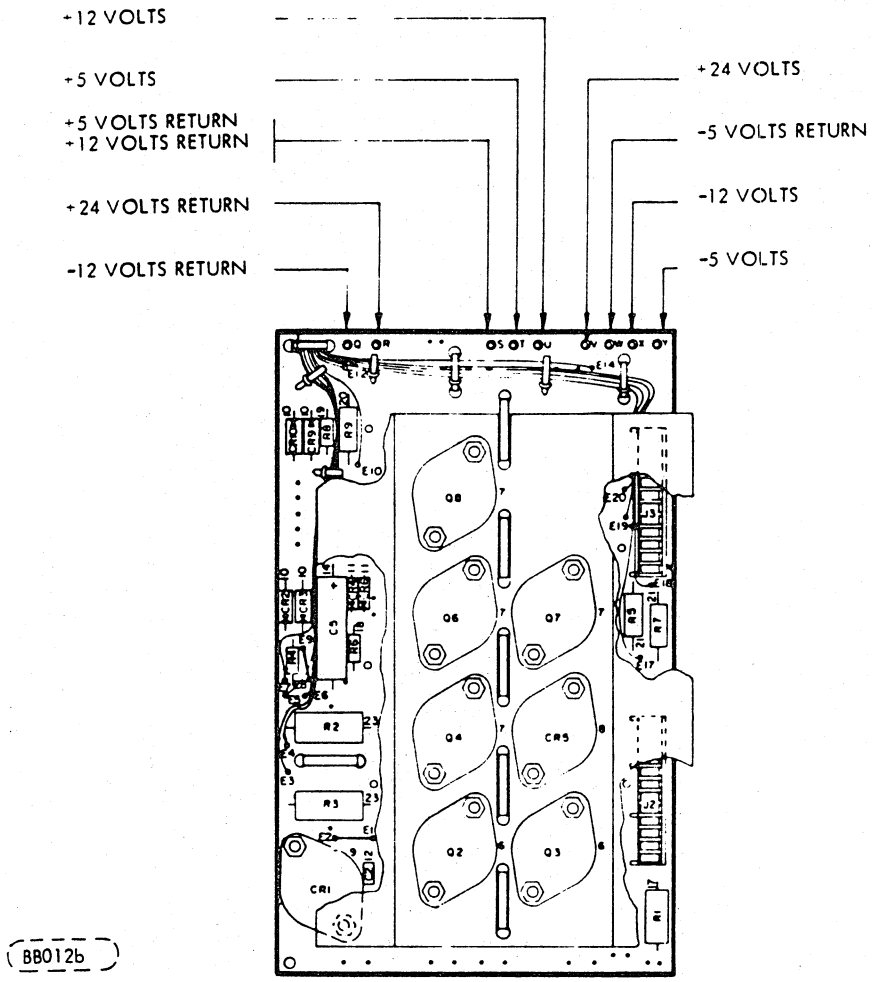


Figure 7-3. Voltage Test Points for Power Supply

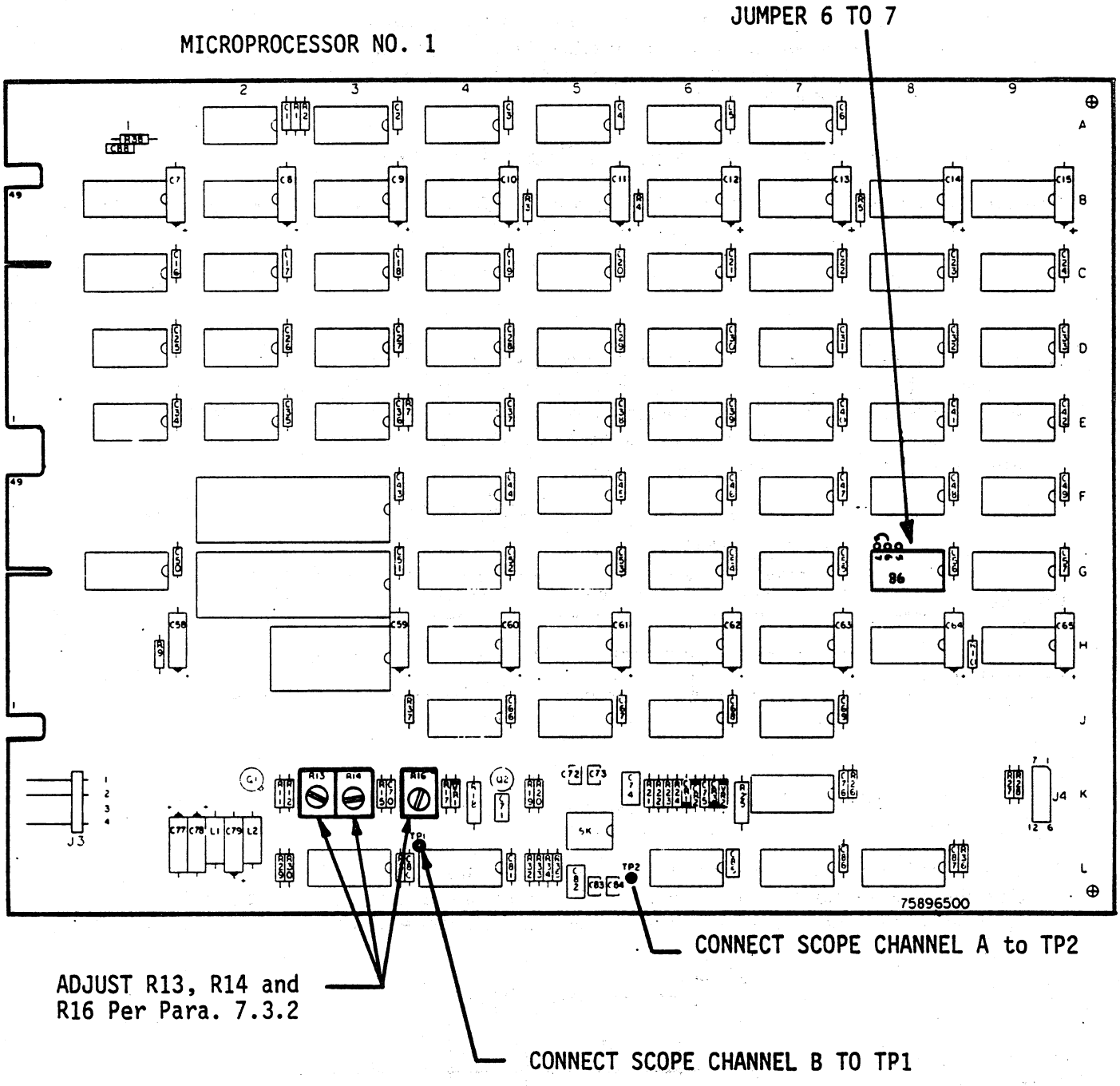


Figure 7-4. Test Procedure for Aligning the Phase Lock Loop

7.3.2 ADAPTER TEST POINTS AND ADJUSTMENTS

Adjustments to the Adapter will be a rare necessity. However, should it be necessary alignment of the phase-lock loop is described below. Should data recovery errors become excessive, an investigation of the phase-lock loop operation as described below may help pinpoint the problem.

7.3.2.1 Procedure for Aligning the Phase-Lock Loop

Equipment needed: Oscilloscope, Diskette with all ones or use header area of preformatted all ones or all zeros.

1. Connect Channel A of the oscilloscope to TP1 of Microprocessor No. 1, and Channel B to TP2. Sync the oscilloscope internally on Channel A. Set the horizontal sensitivity to about 1 us/div and the vertical sensitivity to about 5 volts/div. Load the head and make sure data is displayed on Channel A. A nearly identical signal should appear on B. See Figure 7-5.

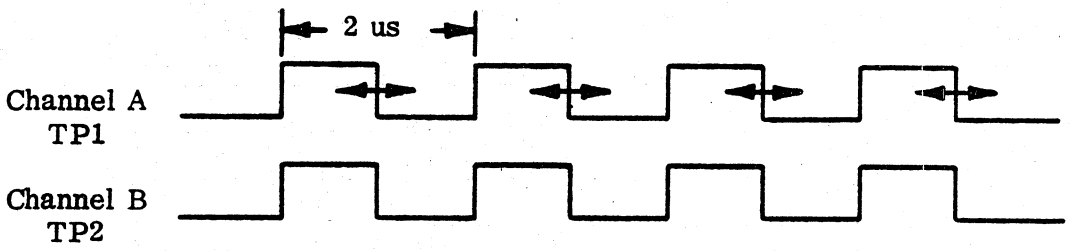


Figure 7-5. Data (A) and VCO (B) Compared

2. Adjust R14 for 1 usec pulses on Channel A. Adjust R16 for the waveform on Channel B to be as shown in Figure 7-5. With the oscilloscope controls invert Channel B and add the two channels. The oscilloscope display should be as in Figure 7-6.

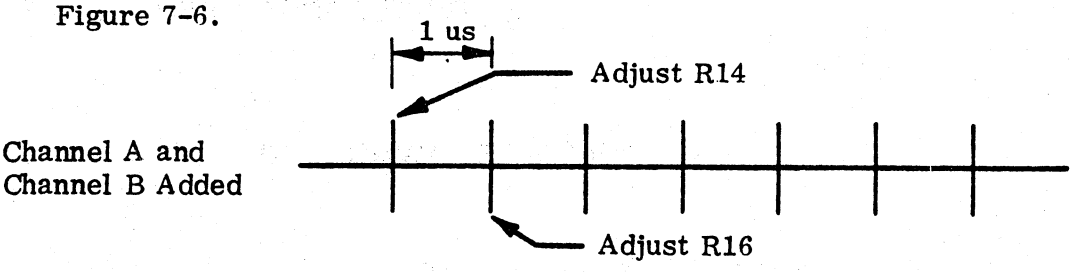


Figure 7-6. Phase Difference Between DF Data (A) and VCO (B)

3. Minimize the width of the spikes of the added signal shown in Figure 7-6 by Adjusting R14 and R16 on Microprocessor No. 1 Board.

4. Set the machine for MFM operation by installing jumper from 8G pin 6 to 8G pin 7. Change Oscilloscope horizontal sensitivity to .5 us per division.

5. Adjust R13 for the picture shown in Figure 7-7.

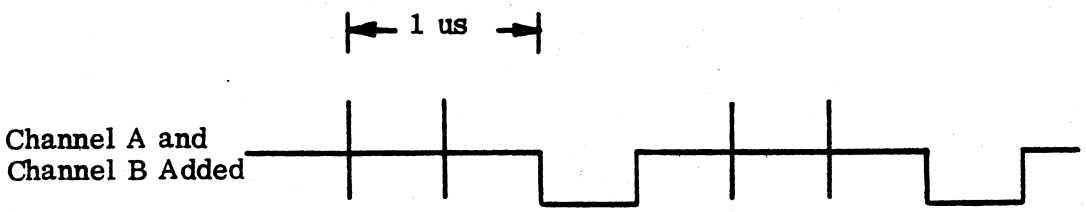


Figure 7-7. Phase Difference Between MFM Data (A) and VCO (B)

6. Mark each adjustable resistor (R13, R14 and R16) with a dob of paint and the board is ready for operation. Remove jumper installed in step 4.

VIII
PARTS

8.1 INTRODUCTION

This section contains drawings and parts lists necessary to provide maintenance and parts replacement support for the FDDS. Assembly breakdown for printed circuit boards are contained in Section 5 with the diagrams.

8.2 GENERAL INSTRUCTIONS

8.2.1 ILLUSTRATIONS

Most figures consist of illustrations depicting a series of parts (kit) as they apply to the FDDS unit. Some figures, such as the Power Supply Figure 8-5 and the Plate Assembly Figure 8-8, illustrates completely replaceable assemblies and parts breakdowns. Others are for pictorial reference only.

8.2.2 TOP LEVEL ASSEMBLY CONFIGURATION

The content of all FDDS variations are listed in Table 8-1. To determine the configuration of the unit with its applicable parts and assemblies, refer to the Top Level and Second Level Configurator Table 8-1. The TLA number of the unit can be found on a sticker at the rear of the unit.

8.2.3 FDD UNIT

Parts data for the FDD Unit used in the FDDS is contained in the appropriate FDD manual supplied with each FDDS Unit. Refer to the Preface page of this manual for identification of the applicable FDD manual.

Table 8-1. FDDS Top and Second Level Configuration Table (Sheet 1 of 2)

FIGURES	FDDS TOP LEVEL ASSY. NO. 778359XX														
		MASTER													
TITLE	NO.	00	01	02	03	04	05	06	07	08	09	10	11	12	13
FDDS COLOR MATRIX	8-1	X	X	X	X	X	X	X	X	X	X	X	X	X	X
STD. OPTION MOUNTING	8-2	△11	△11	△11	△11	△13	△13	△11	△11	△11	△11	△13	△13	△13	△13
STD. LABEL KIT	8-3	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SUB-SYSTEM ASSEMBLY	8-4	△7	△7	△7	△7	△7	△7	△7	△7	△7	△7	△7	△7	△7	△7
POWER SUPPLY **	8-5	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FDD INSTALLATION KIT - MASTER	8-6	△14	△15	△14	△14	△14	△14	△14	△15	△14	△14	△14	△15	△15	△14
PLATE ASSEMBLY **	8-8	△1	△1	△1	△1	△1	△1	△1	△1	△1	△1	△1	△1	△1	△1
PLATE INSTALLATION KIT - MASTER	8-9	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ADAPTER INSTALLATION	8-11	X	X	X	X	X	X	X	X	X	X	X	X	X	X
I/O OPTION	8-12	△3	△3	△3	△3	△3	△3	△16	△16	△3	△3	△3	△3	△3	△3
I/O BRACKET ASSEMBLY - MASTER**	8-13	X	X	X	X	X	X	X	X	X	X	X	X	X	X
HOST I/O CABLE INSTALLATION***	8-15	X	X	X	X	X	X	X	X	X	X	X	X		X
LINECORD	8-16	X	X	X	X	X	X	X	X	X	X	X	X	X	X
JUMPER PLUG *	8-17	△9	△9	△10	△10	△10	△10	△9	△9	△9	△10	△10	△9	△9	△9
SIGNAL RIBBON CABLE FDD-MP BD**	8-18	△5	△5	△5	△5	△5	△5	△5	△5	△5	△5	△5	△5	△5	△5
DC CABLE, I/O PWA TO FDD UNITS**	8-19	X	X	X	X	X	X	X	X	X	X	X	X	X	X
DC CABLE, I/O PWA TO MP BDS**	8-20	X	X	X	X	X	X	X	X	X	X	X	X	X	X
LOGIC CABLE MP 1 to MP 2**	8-21	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SIGNAL RIBBON CABLE - HOST	8-22	X	X	X	X	X	X	X	X	X	X	X	X	X	X
AC POWER CABLE TO FDD UNITS**	8-23	X	X	X	X	X	X	X	X	X	X	X	X	X	X
DUMMY PANEL INSTALLATION	8-25		X	X		X			X				X	X	X

△1 77833950-7
△2 77833951-5
△3 77835150-2 (No. 1)
△5 77835240-1
△6 77835241-9
△7 75884725-5
△14 77835156-9
△8 75884726-3
△9 77830722-3
△10 77830724-9
△15 75880251-6
△11 77833850-9
△12 77833851-7
△13 77833852-5
△16 77614552-6 (No. 3)

*SEE FIGURE 3-3 FOR JUMPER CONFIGURATIONS REQUIRED.
**THESE ITEMS ARE NOT CALLED OUT ON THE TLA BUT ARE SECOND LEVEL DRAWINGS (CALLED OUT BY DRAWINGS ON THE TLA).
***USED ONLY IF HOST IS EXTERNAL TO FDDS CABINET.

XX058a

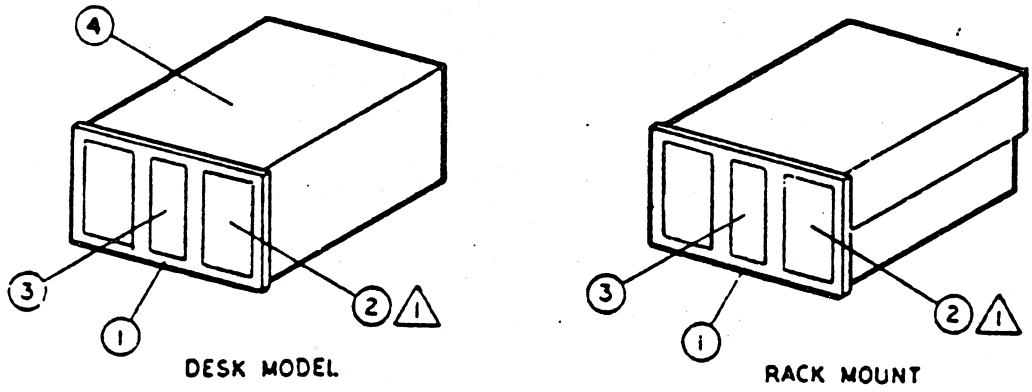
Table 8-1. FDDS Top and Second Level Configuration Table (Sheet 2 of 2)

FIGURES	FDDS TOP LEVEL ASSY. NO. 778359XX																
		SLAVE															
TITLE	NO.	50	51	52	53	54											
FDDS COLOR MATRIX	8-1	X	X	X	X	X											
STD. OPTION MOUNTING	8-2	△11	△11	△11	△11	△13											
STD. LABEL KIT	8-3	X	X	X	X	X											
SUB-SYSTEM ASSEMBLY	8-4	△8	△8	△8	△8	△8											
POWER SUPPLY **	8-5	X	X	X	X	X											
FDD INSTALLATION KIT - SLAVE	8-7	X	X	X	X	X											
PLATE ASSEMBLY **	8-8	△2	△2	△2	△2	△2											
PLATE INSTALLATION KIT - SLAVE	8-10	X	X	X	X	X											
I/O OPTION	8-12	△4	△17	△4	△4	△4											
I/O BRACKET ASSEMBLY - SLAVE**	8-14	X	X	X	X	X											
LINECORD	8-16	X	X	X	X	X											
JUMPER PLUG *	8-17	△9	△9	△9	△10	△10											
SIGNAL RIBBON CABLE FDD/MP BD**	8-18	△6	△6	△6	△6	△6											
DC CABLE, I/O PWA TO FDD UNITS**	8-19	X	X	X	X	X											
AC POWER CABLE TO FDD UNITS**	8-23	X	X	X	X	X											
FDDS MASTER TO SLAVE INTERCONN	8-24	X	X	X	X	X											
DUMMY PANEL INSTALLATION	8-25																

△1 77833950-7
△2 77833951-5
△4 77835155-1(No 2)
△5 77835240-1
△6 77835241-9
△7 75884725-5
△14 77835156-9
△8 75884726-3
△9 77830722-3
△10 77830724-9
△15 75880251-6
△11 77833850-9
△12 77833851-7
△13 77833852-5
△17 77614553-4 (No.4)

*SEE FIGURE 3-3 FOR JUMPER CONFIGURATIONS REQUIRED.
**THESE ITEMS ARE NOT CALLED OUT ON THE TLA BUT ARE SECOND LEVEL DRAWINGS (CALLED OUT BY DRAWINGS ON THE TLA).

XX252a

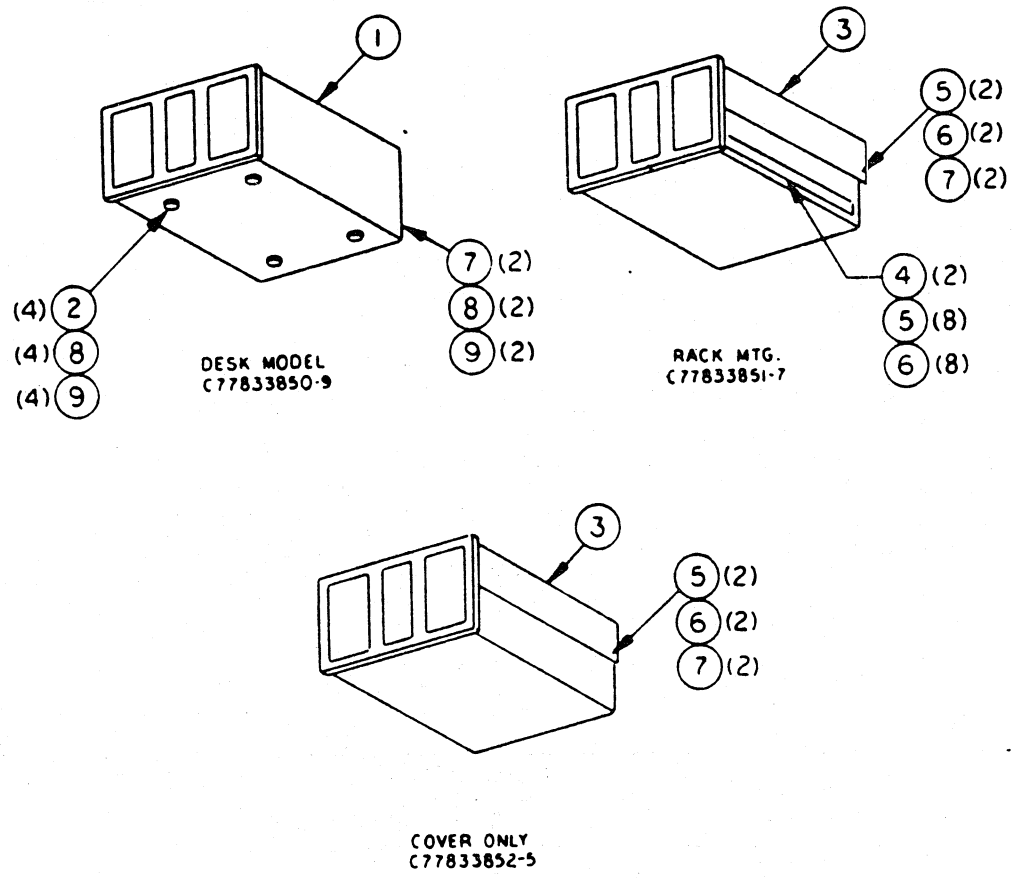


△1. FDD FRONT PLATE OR DUMMY PANEL.
Table 8-1 defines usage (Figure 8-25).

COLOR MATRIX	ITEM NUMBER					
	1	2	3	4A	4B	4C
77834801-1	X	X	X	X		
77834802-9	X	X	X			X
77834803-7	X	X	X			
77834804-5	X		X	X		
77834805-2	X		X			X
77834806-0	X		X			

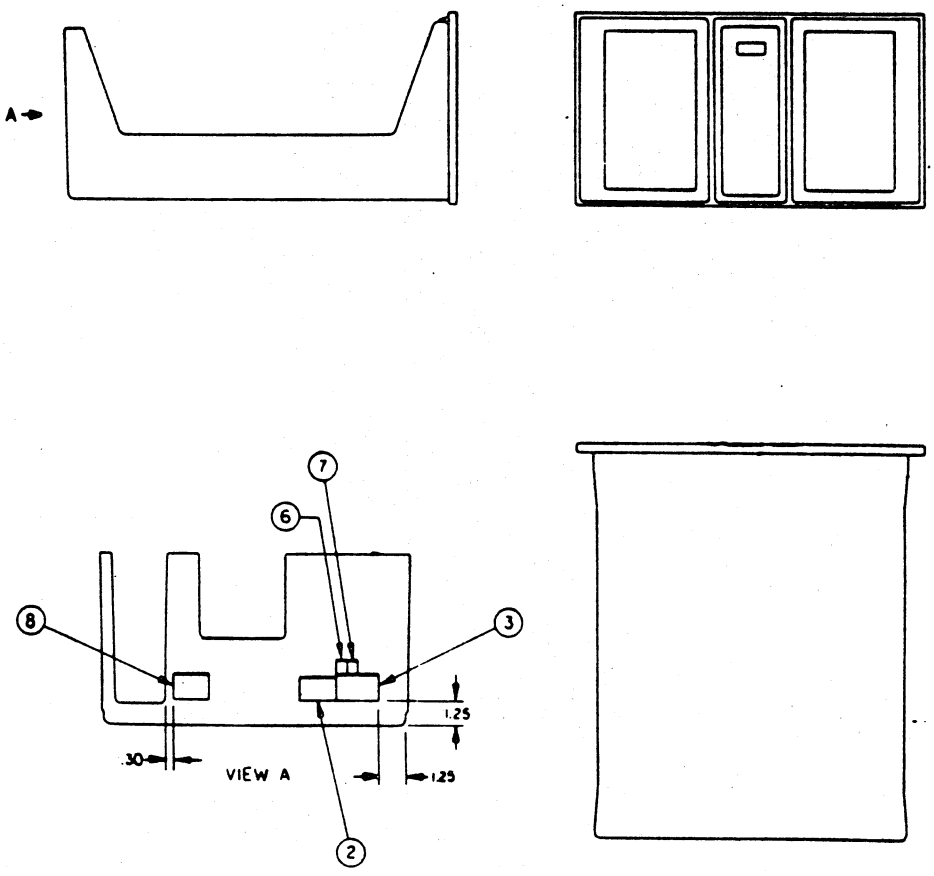
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77834800-3	FDDS Color Matrix	See table above for applicable parts
1	77580401-6	Chassis	See Figure 8-25
2	77834902-7	Panel Assembly	See Figure 8-8
3	83431901-4	Plate-Air Inlet	
4A	83430701-9	Cover	
4B	83430702-7	Cover	
4C	83430703-5	Cover	

Figure 8-1. FDDS Color Matrix



ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77833850-9	Std Option Mtg	See illustration for application of parts
	77833851-7	Std Option Mtg	
	77833852-5	Std Option Mtg	
1	83430700-1	Cover	
2	83430200-2	Foot-Mount	
3	83430800-9	Cover	
4	94251000-0	Slide	
5	10127123-7	Screw	
6	10126104-8	Lk Washer	
7	10125607-1	Washer	
8	10127133-6	Screw 10-2	
9	10126105-5	Lk Washer #10	

Figure 8-2. Standard Option Mounting



ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77833825-1	Std Label Kit	
	77833826-9	Std Label Kit	
	77833827-7	Std Label Kit	
2	77832696-7	Label Ident/Rating	
3	77830778-5	Label, volts	
6	77830537-5	Label UL	On 77833825 only
7	77830538-3	Label CSA	On 77833825, 77833826 only
8	24547531-4	Label, Caution	

Figure 8-3. Standard Labeling Installation Kit

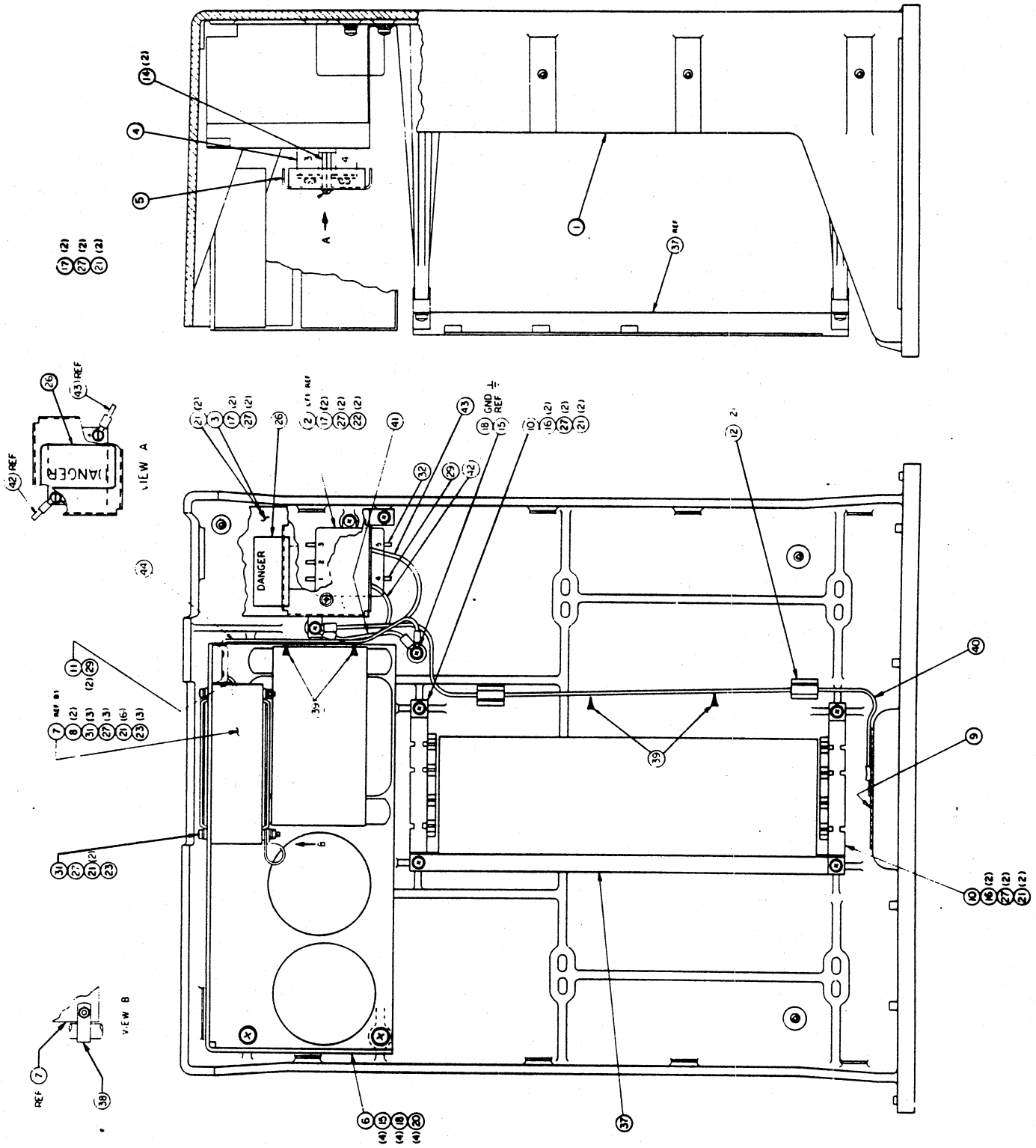


Figure 8-4. Sub-System Assembly - (Sheet 1 of 2)

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	75884725-5	Module Assembly, Master	
	75884726-3	Module Assembly, Slave	
1	77580400-8	Chassis	
2	62071531-8	Filter	
3	75884582-0	Enclosure-Filter	
4	95689301-0	Relay	
5	75884695-0	Cover-Relay	
6	76835500-8	Power Supply	
7	83464100-3	Fan	
8	83464103-7	Grille-Fan	
9	77580600-3	Screen-Air Inlet	
10	77830603-5	Cardguide	75884725 Only
11	75275311-1	Cable Assembly	
12	51853006-8	Clamp, Cable Adhesive	
13	94277419-1	Strap, Cable Tie	75884725 Only
14	51673807-7	Spacer, 6-32X1 Hex	
15	10127132-8	Scr Pan Hd Mach 10-2	
16	10127116-1	Scr Pan Hd 6-32	75884725 Only
17	10127114-6	Scr Pan Hd 6-32X1/2	
18	10126105-5	Wash Int Tooth Lk #10	
20	10125607-1	Washers Plain 10	
21	10125605-5	Washers Plain 6	
22	94279109-6	Washer	
23	10125105-6	Nut Hex Mach 6-32	
26	24547501-7	Plate Warning	
27	10126401-8	Washers Ext Tooth Lo	
29	93541016-7	Terminal, Ring Tongue	
31	92742182-6	Screw Pan Hd 632X2 1/4	
32	93541017-5	Terminal, Ring Tongue	
37	77830887-4	Plate Assembly, PWA	75884725 Only
38	92602007-4	Clamp, Cable	
39	94277400-1	Strap, Cable Tie	
40	75887050-5	Wire Assembly	
41	75887051-3	Wire Assembly	
42	75887052-1	Wire Assembly	
43	75887053-9	Wire Assembly	
44	75887055-4	Wire Assembly	
45	75887054-7	Wire Assembly	
46	75887056-2	Wire Assembly	

Figure 8-4. Sub-System Assembly - (Sheet 2 of 2)

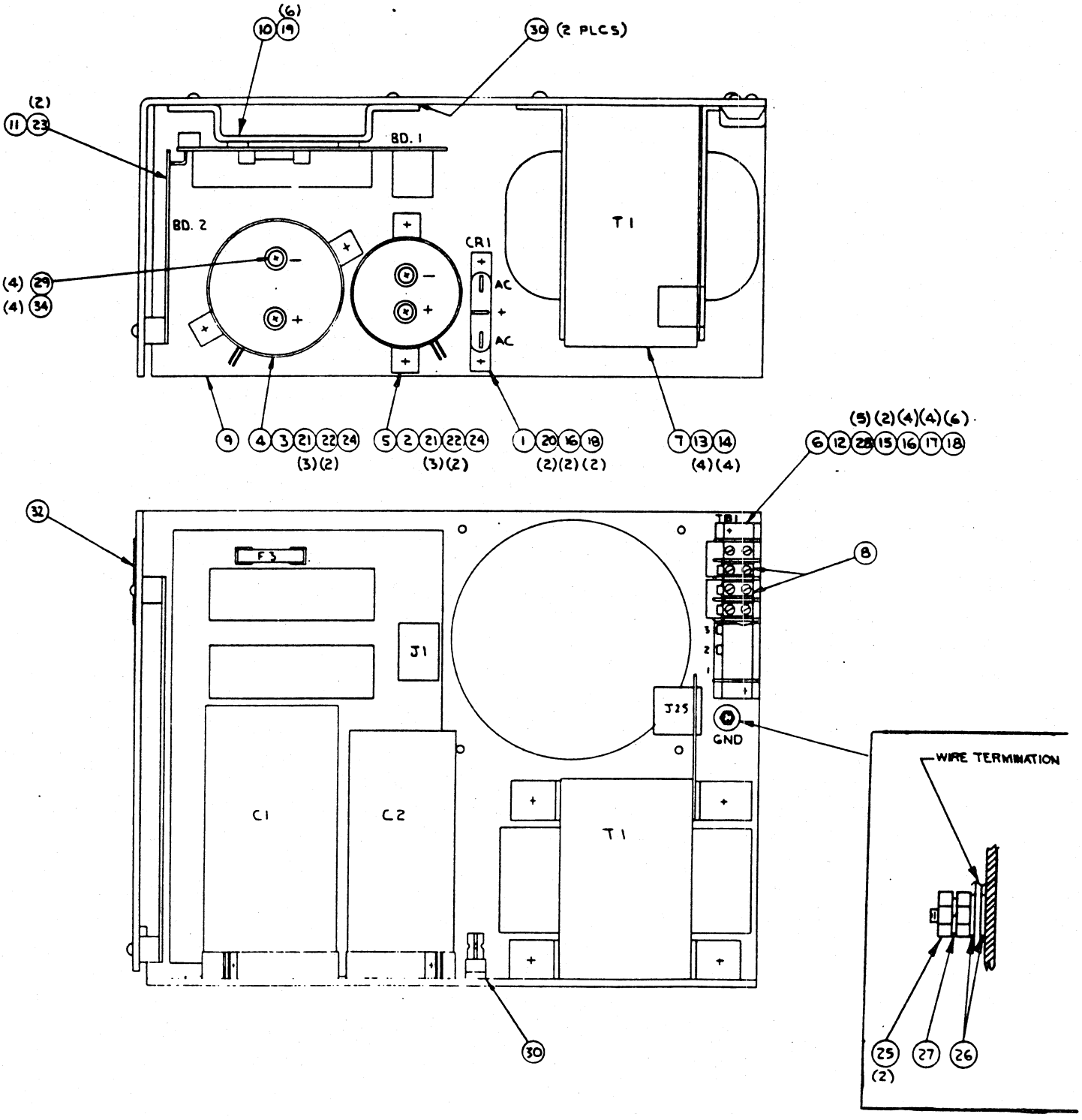
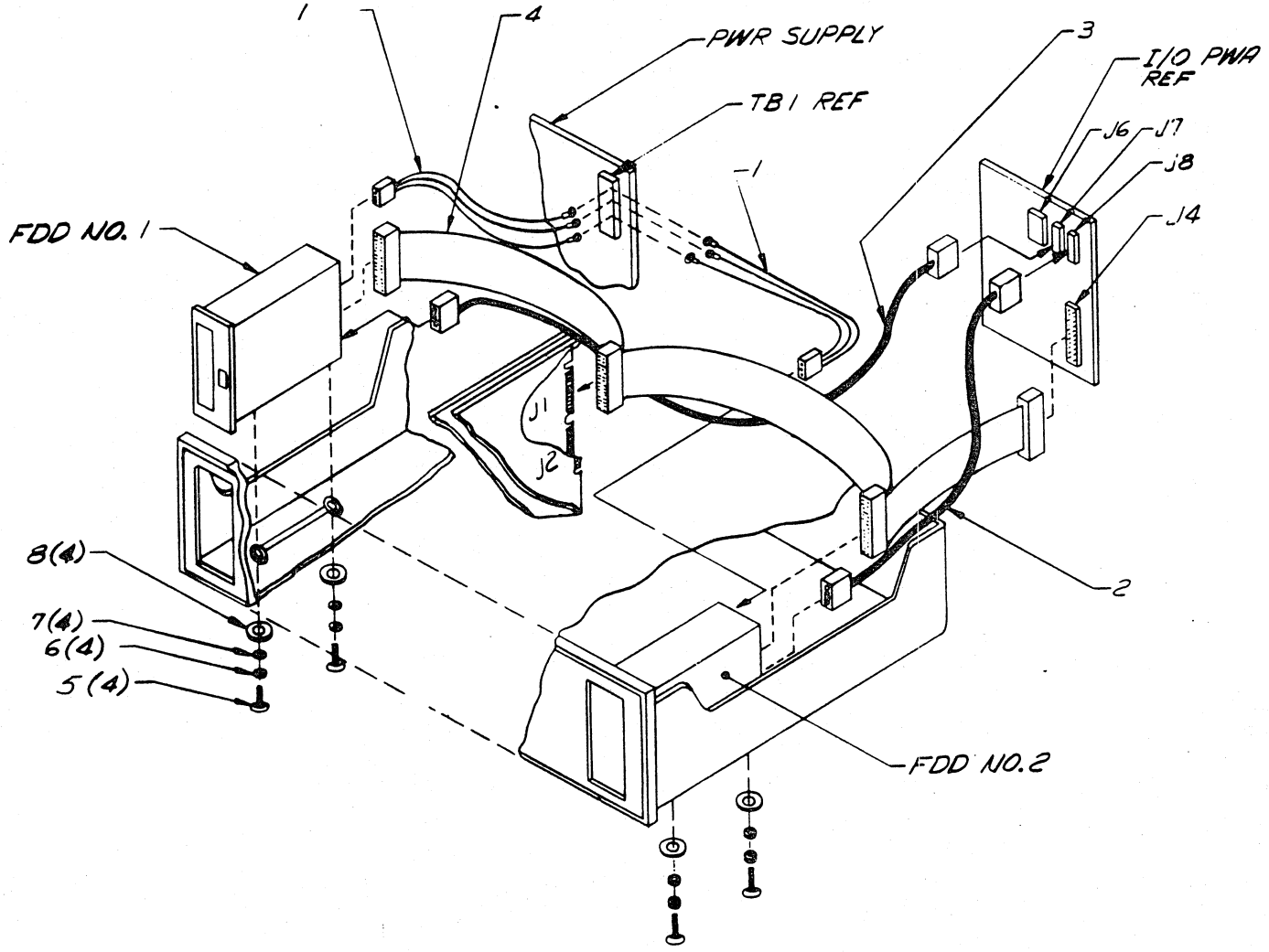


Figure 8-5. Power Supply - (Sheet 1 of 2)

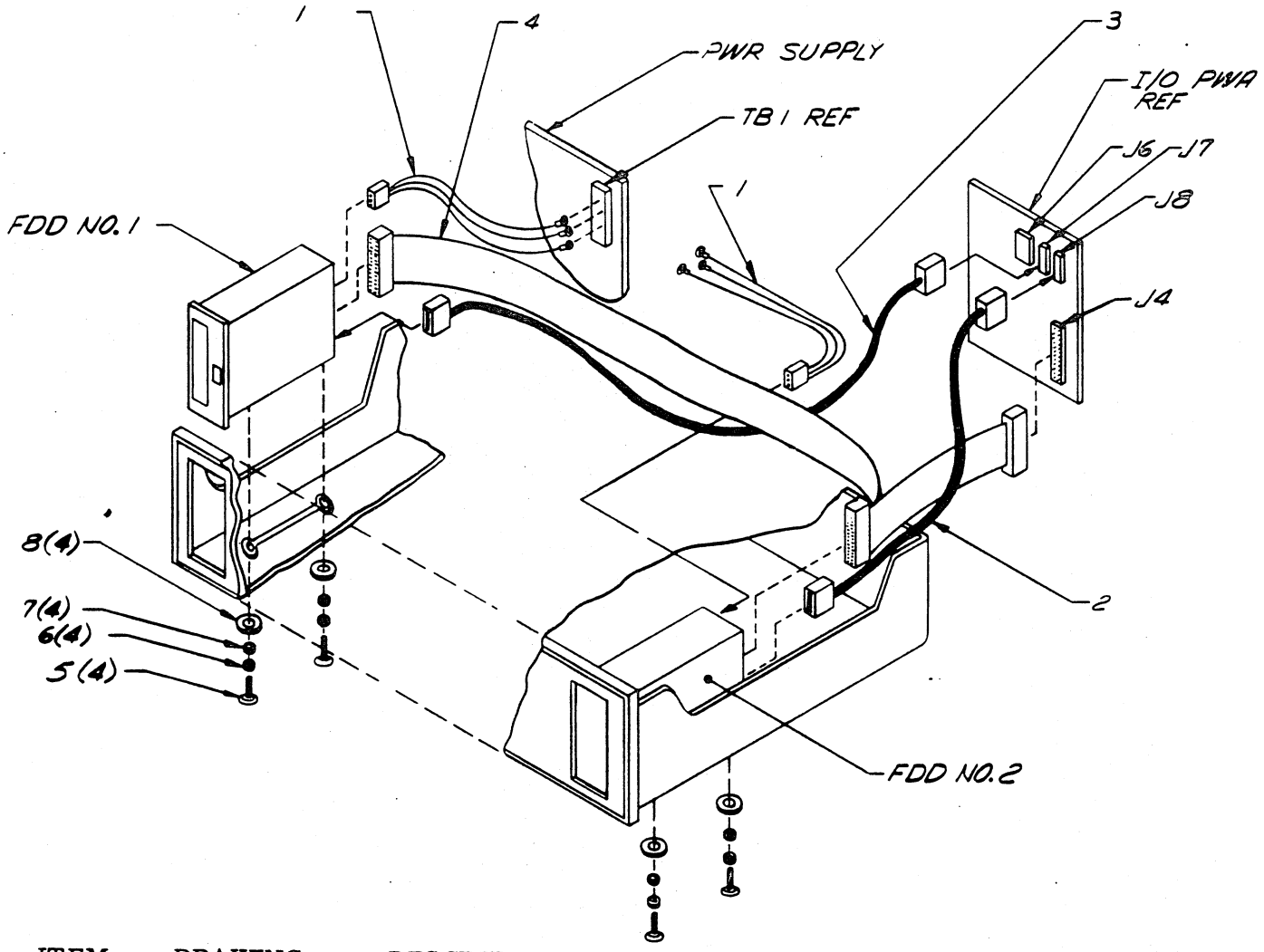
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	76835500-8	Power Supply	
1	95583505-3	Rectifier Block 15A	
2	92691009-2	Clamp, Capacitor Mtg	
3	92691011-8	Clamp, Capacitor Mtg	
4	95661312-9	Capacitor, 15 VDC 110000 Mfd	
5	95642307-3	Cap 40 VDC 30000 Mfd	
6	95689507-2	Terminal Strip Barrier	
7	76842100-0	Transformer Linear	
8	56093802-9	Jumpers	
9	76844300-4	Chassis	
10	76845000-9	Type GVYN Comp Assy	
11	76845400-1	Type GVZN Comp Assy	
12	76791500-2	Cover-Terminal Strip	
13	95634808-0	Speed Nut-U Type	
14	95655556-9	Screw, 1/4 x 14	
15	10127118-7	Screw 6-32X1	
16	10125803-6	Washers Lock 6	
17	10125613-9	Washers 6	
18	95510026-8	Nut, Hex Screw	
19	17901523-5	Scr 10-32X3/8	
20	10125716-0	Scr Flat 6-32X	
21	95634801-5	Speed Nut-U	
22	95655416-6	Screw, Flt Hd	
23	95655534-6	Screw, 1x8/18	
24	95655517-1	Screw 6-20x1/2	
25	10125108-0	Nut-Hex Screw	
26	10126403-4	Washers Lock	
27	10125805-1	Washers Lock	
29	10127143-5	Screw 10-32x1/2	
32	95797855-4	Plate Ident	
34	95524402-5	Washer, Lock	

Figure 8-5. Power Supply - (Sheet 2 of 2)



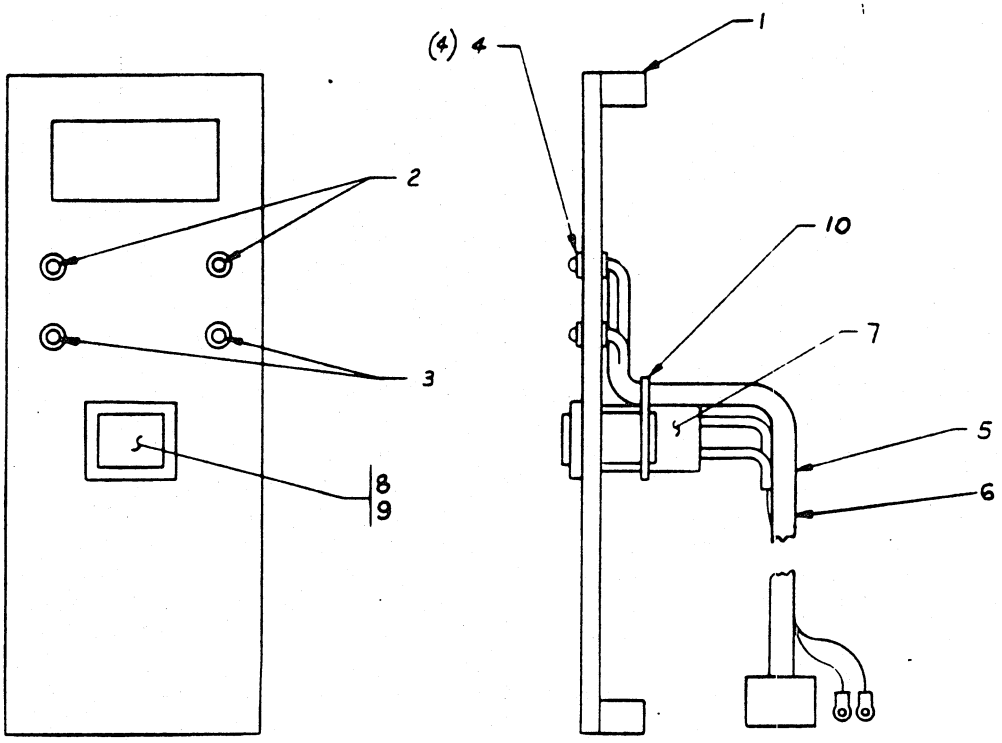
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	75880251-6	FDD Installation Kit - Master	
	77835156-9	FDD Installation Kit - Master	
1	77832220-6	AC Cable	
2	77835244-3	DC Cable, FDD	TLA Tabs 00, 03, 05, 06, 08, 09
3	77835245-0	DC Cable, FDD	
4	77835240-1	Signal Rbn Cbl-FDD	
5	10127137-7	Screw #10-24	
6	10126403-4	Washers Ext Tooth Lock	
7	10125607-1	Washers Plain 10	
8	10125608-9	Washers Plain 1/4	

Figure 8-6. FDD Installation - Master



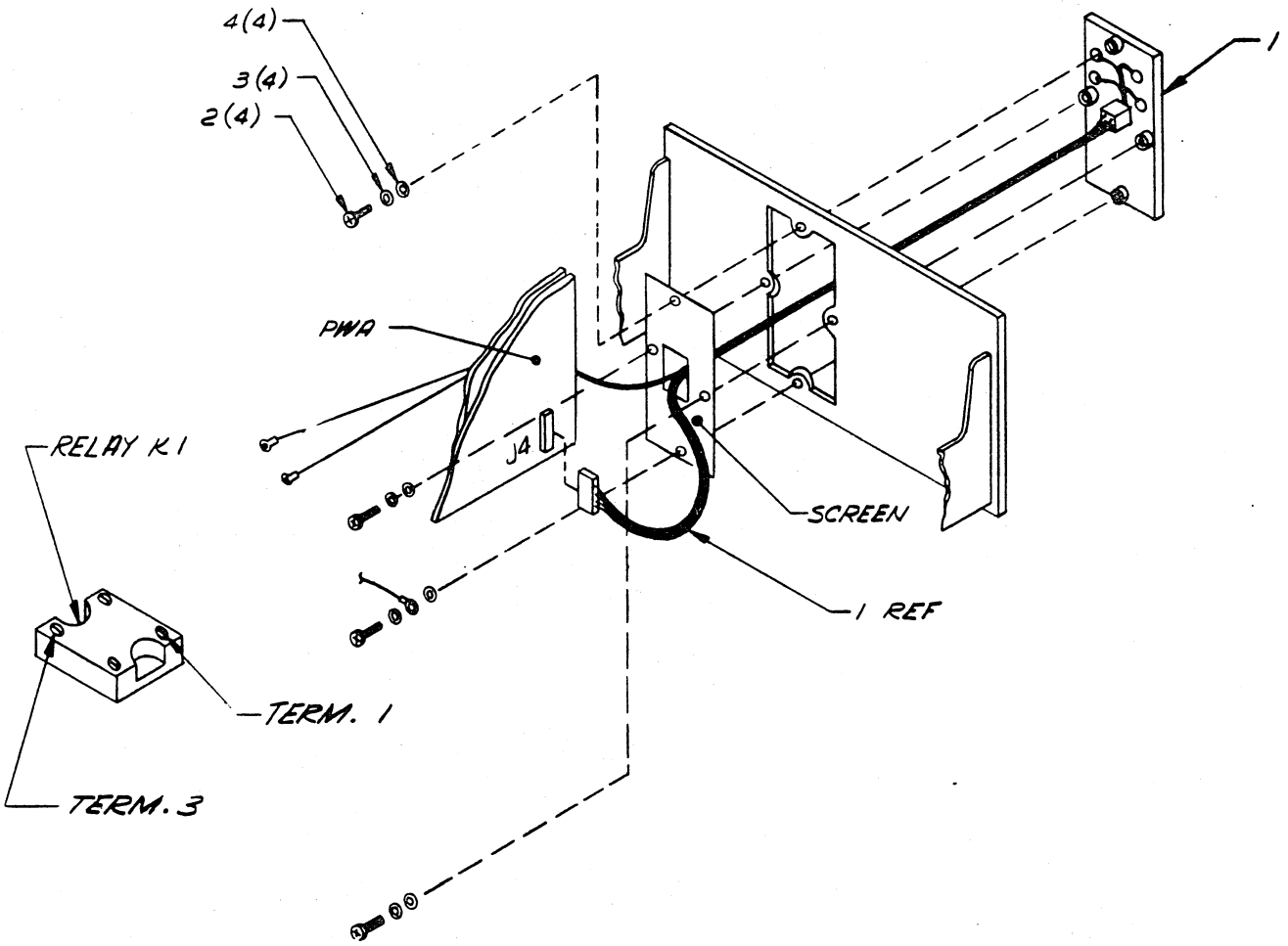
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77835157-7	FDD Installation Kit - Slave	
1	77832220-6	AC Cable	
2	77835244-3	DC Cable, FDD	TLA Tabs 50, 51, 52, 53, 54
3	77835245-0	DC Cable, FDD	
4	77835241-9	Signal Rbn Cbl-FDD	
5	10127137-7	Screw #10-24	
6	10126403-4	Washers Ext Tooth Lock	
7	10125607-1	Washers Plain 10	
8	10125608-9	Washers Plain 1/4	

Figure 8-7. FDD Installation Kit - Slave



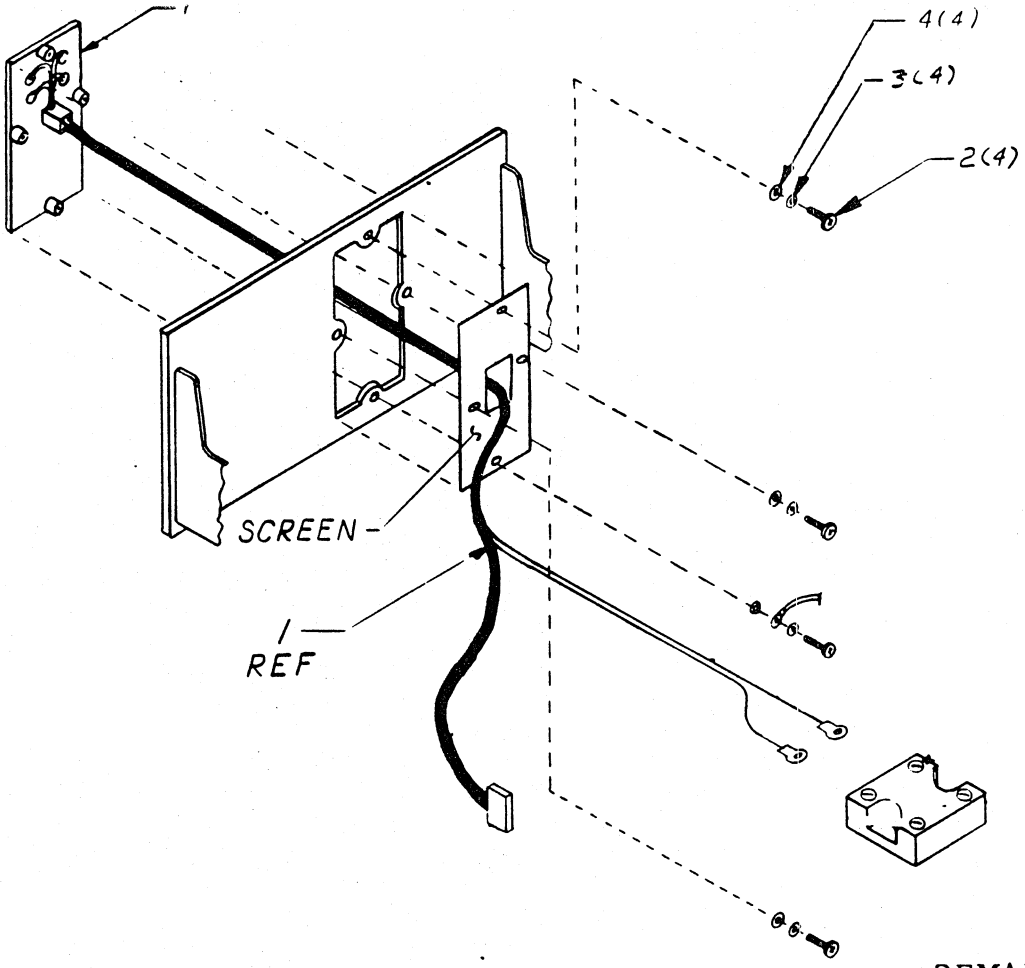
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77833950-7	Plate Assembly	See Figure 8-9
	77833951-5	Plate Assembly	See Figure 8-10
1	83431901-4	Plate-Air Inlet	
2	75810701-5	LED	
3	83464600-2	LED	
4	75810703-1	LED Retainer	
5	77581701-8	Cable Assembly-LED	77833950-7 (Master)
6	77581702-6	Cable Assembly-LED	77833951-5 (Slave
7	94380301-5	Power Switch	
8	94380400-5	Lamp	
9	94380509-3	Lend	
10	94277417-5	Strap-Cable Tie	

Figure 8-8. Plate Assembly



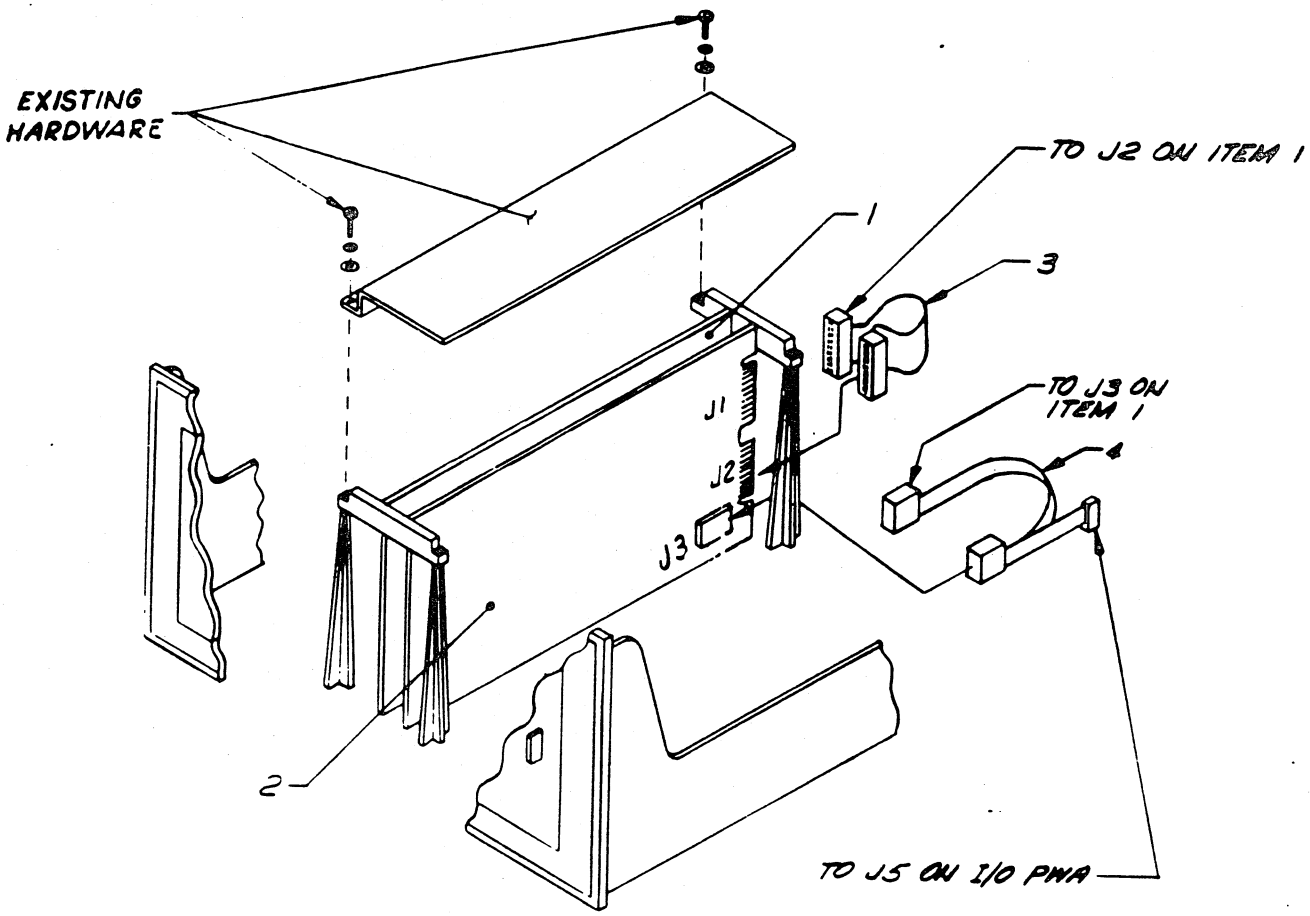
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	75884736-2	Plate Installation Kit	Master
1	77833952-3	Plate Assembly	
2	10127115-3	Screw Pan Hd Mach	
3	10126103-0	Wash Int Tooth Lk #6	
4	10125605-5	Washers Plain 6	

Figure 8-9. Plate Installation Kit - Master



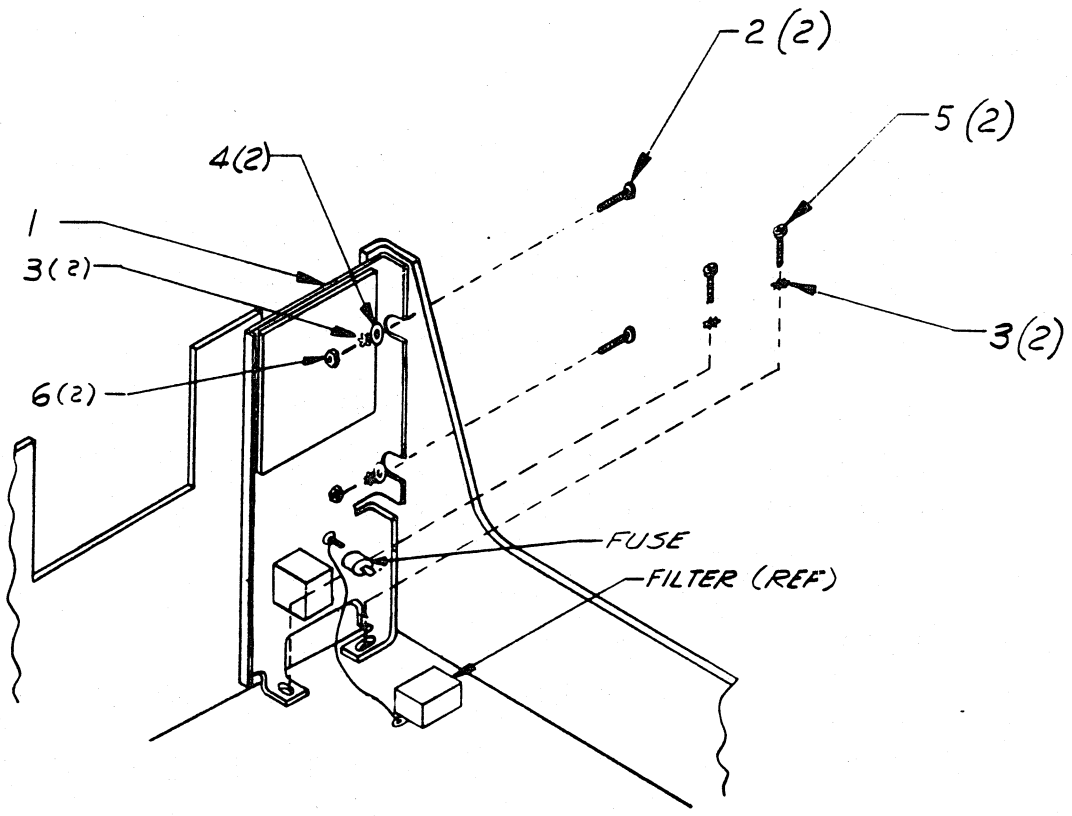
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	75884735-4	Plate Installation Kit	Slave
1	77833951-5	Plate Assembly	
2	10127115-3	Screw Pan Hd Mach	
3	10126103-0	Wash Int Tooth Lk #6	
4	10125605-5	Washer Plain 6	

Figure 8-10. Plate Installation Kit - Slave



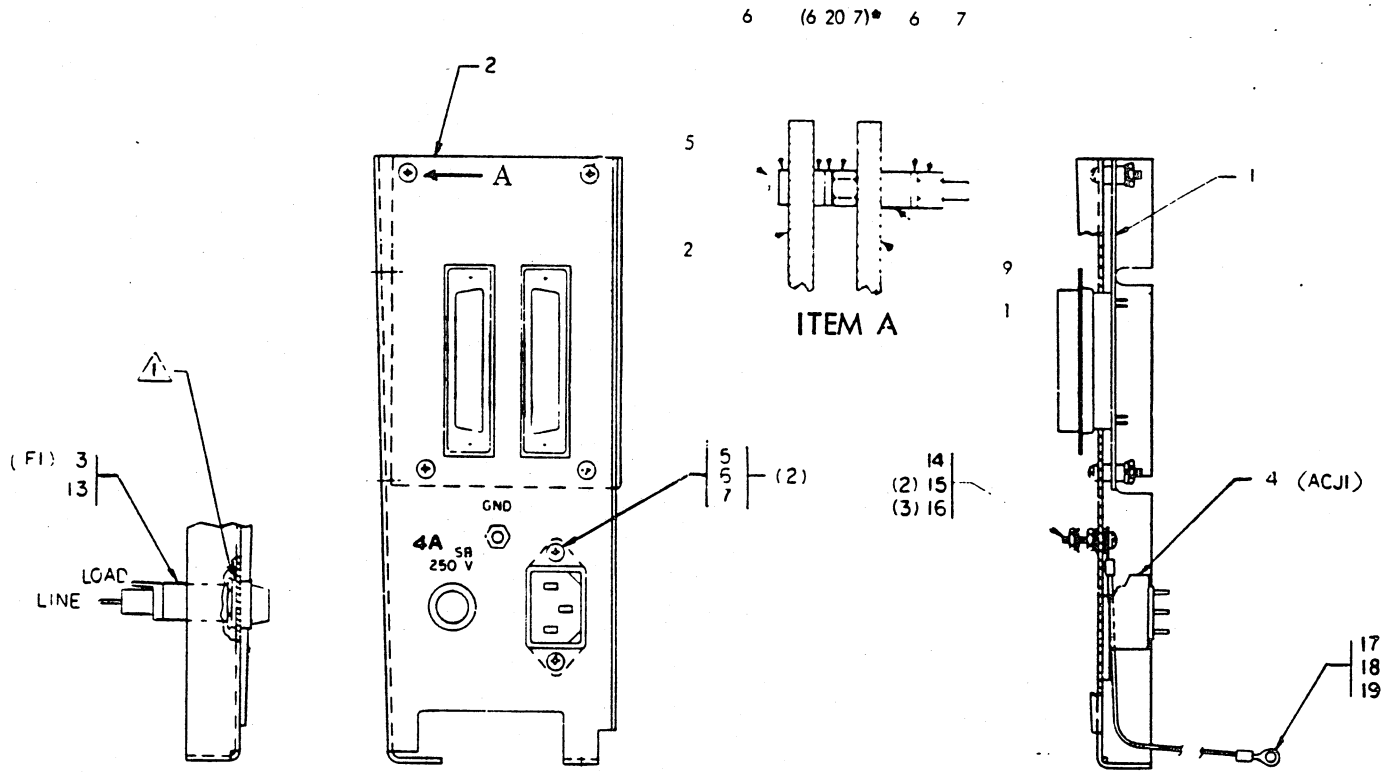
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	75897100-6	Adapters FDDS Master	
1	75896500-8	Micro Proc PWA #1	See Section 5
2	75896602-2	Micro Proc PWA #2	for breakdown
3	77835247-6	Signal Ribbon Cable Jump	
4	77835246-8	DC Cable, Signal	

Figure 8-11. Adapter Installation



ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77835150-2	I/O Option No. 1	(Master)
	77835155-1	I/O Option No. 2	(Slave)
	77614552	I/O Option No. 3	(Master)
	77614553	I/O Option No. 4	(Slave)
1	77836060-2	Bracket Assy I/O, Master (No. 1)	(Figure 8-13)
1	77836061-0	Bracket Assy I/O, Slave (No. 2)	(Figure 8-14)
1	77614550	Bracket Assy I/O, Master No. 3)	(Fig. 8-13)
1	77614551	Bracket Assy I/O, Slave (No. 4)	(Fig. 8-14)
2	10127133-6	Screw Pan Hd Mach 10-2	
3	10126403-4	Washer Ext Tooth Lock	
4	10125607-1	Washers Plain 10	
5	10127132-8	Screw Pan Hd Mach 10-2	
6	10125107-2	Nut-Hex Mach-10	

Figure 8-12. I/O Option

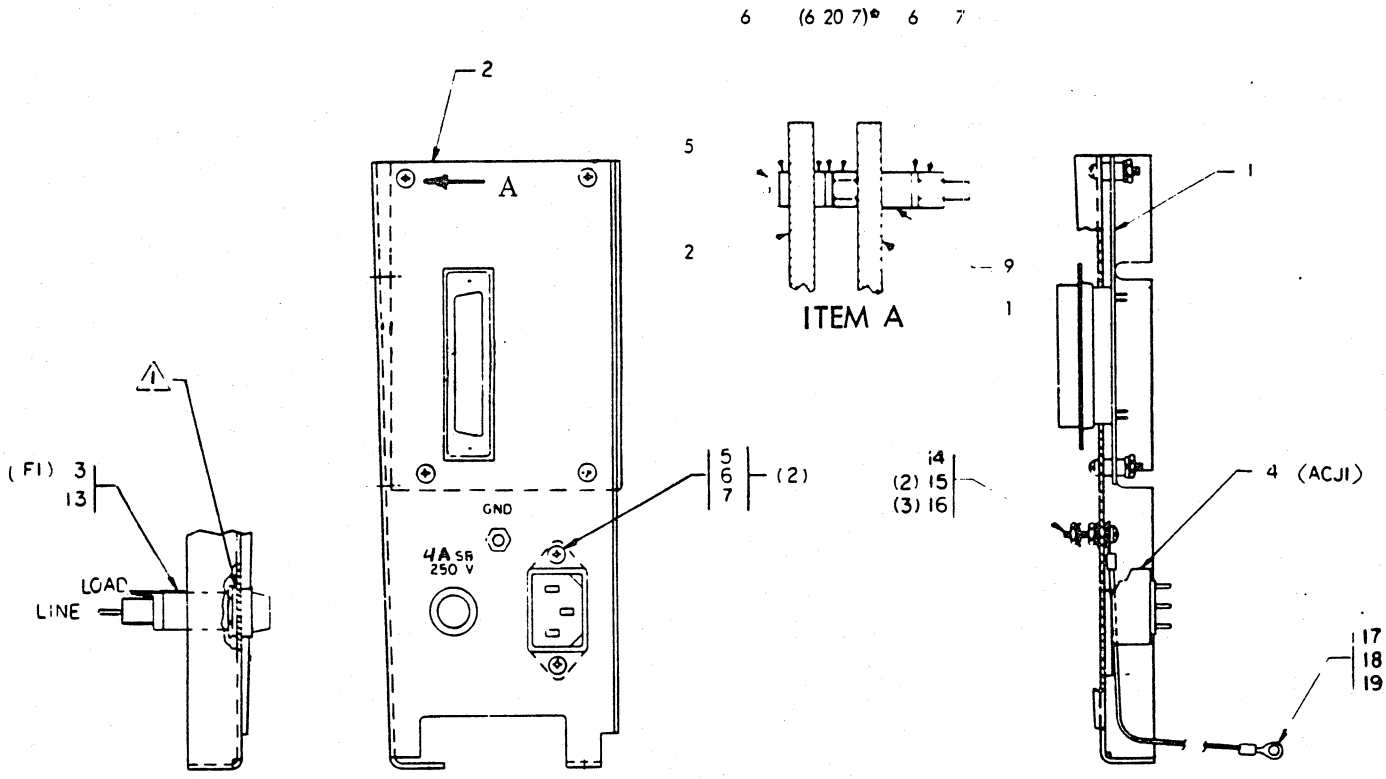


ITEM	DRAWING	DESCRIPTION	REMARKS
	77836060-2	I/O Bracket Assy (No. 1)	(Master)
	77614550-0	I/O Bracket Assy (No. 3)	(Master)
1	77834600-7	PWA I/O No. 1	Used on 77836060
1	75895750	PWA I/O No. 3	Used on 77614550
2	77835242-7	Bracket-I/O	
3	95598800-1	Fusehldr Quick-Conn	
4	51870400-2	AC Pwr Receptacle	
5	10127115-3	Screw Pan Hd Mach	
6	10126103-8	Wash Int Tooth Lk #6	
7	10125105-6	Nut Hex Mach 6-32	
9	51760015-1	Spacer	
13	75885068-9	Fuse, Slow Blowing	
14	10127144-3	Scr Pan Hd 10-32	
15	10125108-0	Nut Hex Mach 10-32	
16	10126403-4	Washers Ext Tooth Lock	
17	15003254-8	Wire, Elec 16 Ga	
18	93541016-7	Terminal, Ring Tongue	
19	93541018-3	Terminal, Ring Tongue	
20	10125605-5	Washer Plain	

⚠1 NOTE: Washer furnished with Item 3, Fuse Holder

*Only I/O Bracket Assy No. 3 Uses Items 6, 20, 7 here.
I/O Bracket Assy No. 1 Uses Item 9, Spacer instead.

Figure 8-13. I/O Bracket Assembly (Master)

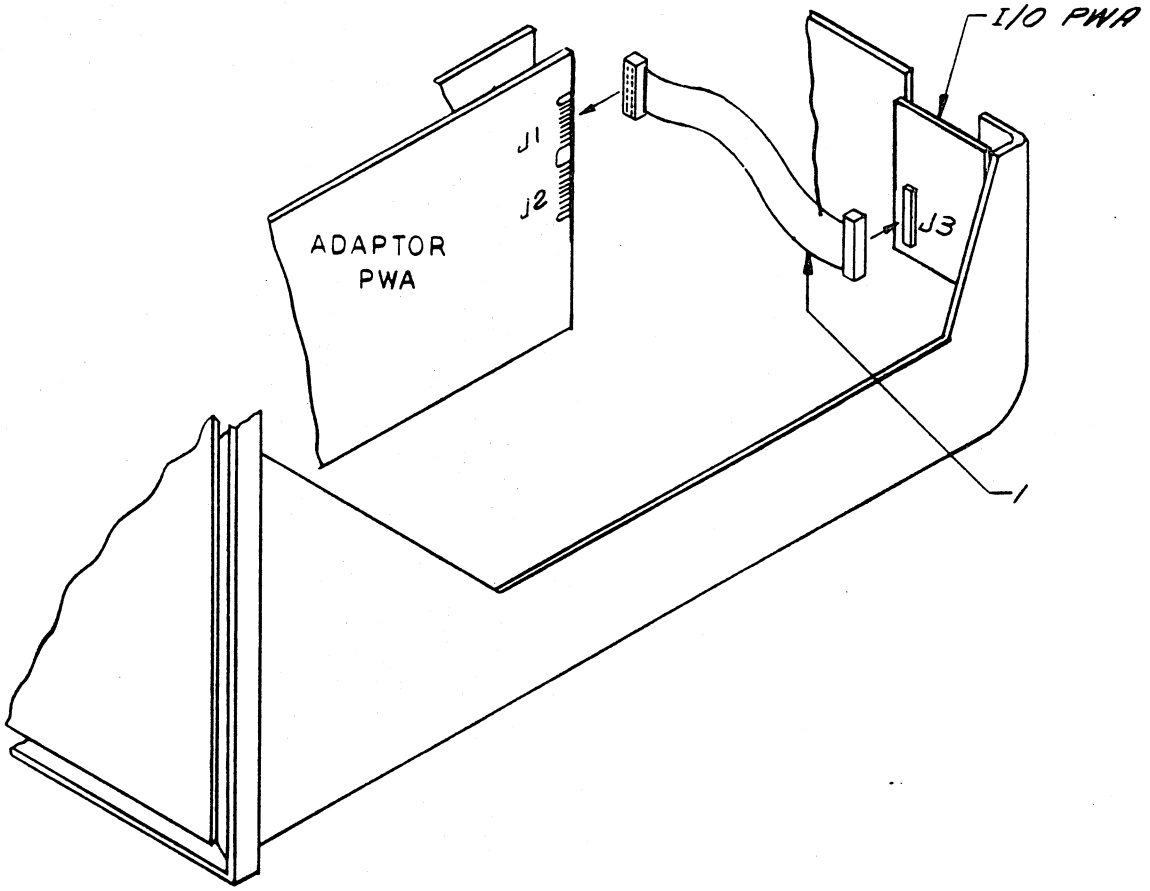


ITEM	DRAWING	DESCRIPTION	REMARKS
	77836061	I/O Bracket Assy (No. 2)	(Slave)
	77614551	I/O Bracket Assy (No. 4)	(Slave
1	77834450-7	PWA I/O No. 2	Used on 77836061
1	75895800	PWA I/O No. 4	Used on 77614551
2	77835243-5	Bracket-I/O	
3	95398000-1	Fusehldr Quick-Conn	
4	51870400-2	AC Pwr Receptacle	
5	10127115-3	Screw Pan Hd Mach	
6	10126103-0	Wash Int Tooth Lk #6	
7	10125105-6	Nut Hex Mach 6-32	
9	51760015-1	Spacer	
13	7588506 8-9	Fuse, Slow Blowing	
14	10127144-3	Screw Pan Hd 10-32	
15	10125108-0	Nut Hex Mach 10-32	
16	10126403-4	Washers Ext Tooth Lock	
17	15003254-8	Wire, Elect 16 Ga	
18	93541016-7	Terminal, Ring Tongue	
19	93541018-3	Terminal, Ring Tongue	
20	10125605-5	Washer Plain	

⚠1 NOTE: Washer furnished with Item 3, Fuse Holder.

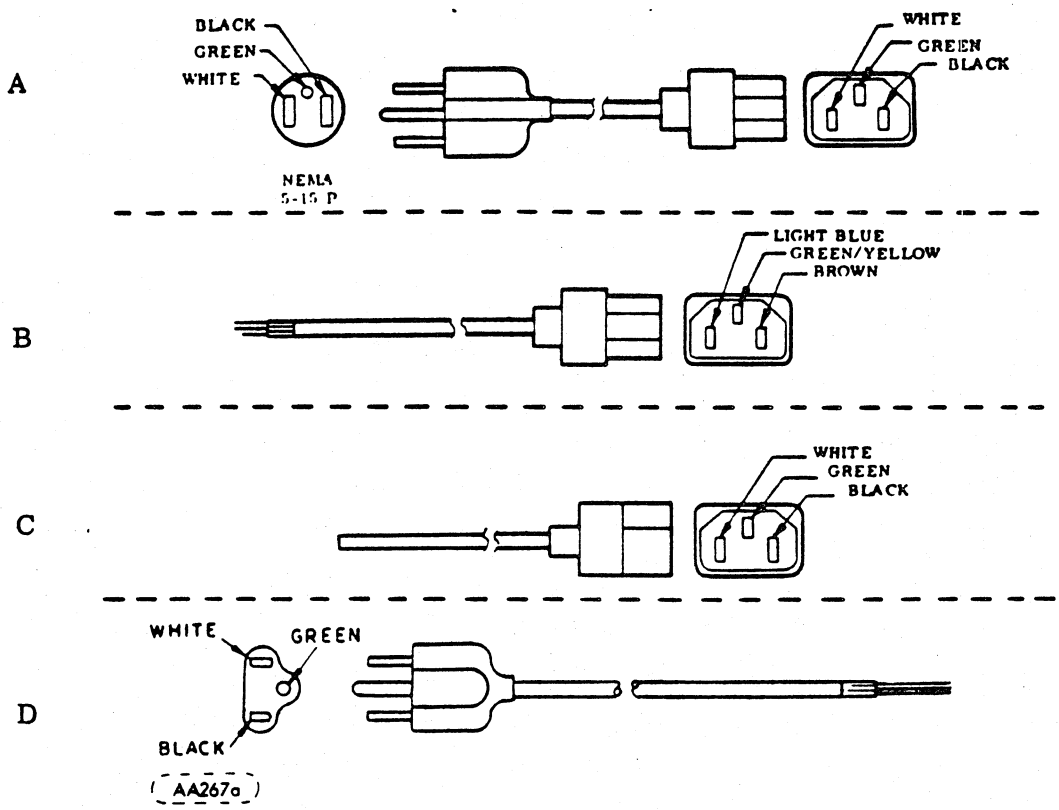
*Only I/O Bracket Assy No. 4 uses Items 6, 20, 7 here.
I/O Bracket Assy No. 2 uses Item 9, Spacer instead.

Figure 8-14. I/O Bracket Assembly (Slave)



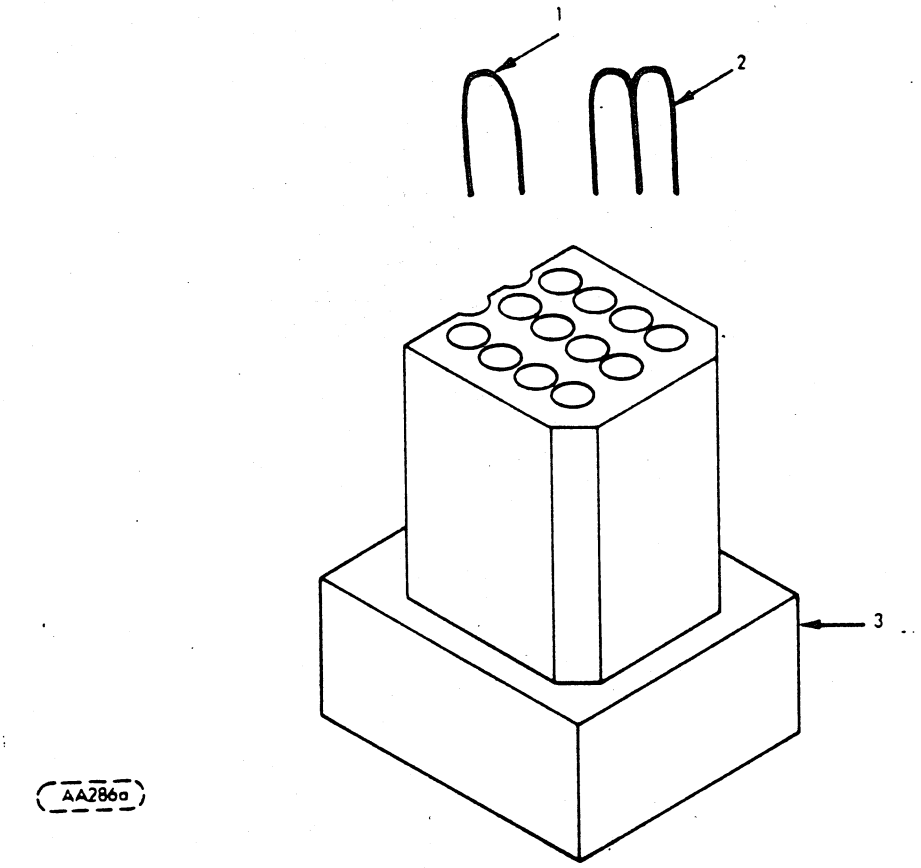
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
		Host I/O Cable Instl Kit	
1	77835248-4	Signal Ribbon Cable Assembly - Host	Refer to Figure 8-22

Figure 8-15. Host I/O Cable Installation



ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS (Used On)
A	75778701-5	125V RMS, 13 Amp, 7 1/2 ft (2.3 m)	00, 01, 06, 07, 08, 11, 12, 13
A	75778702-3	125V RMS, 10 Amp, 7 1/2 ft (2.3 m)	50, 51, 52
B	75778710-6	250V RMS, 10 Amp, 7 1/2 ft (2.3 m)	
B	75778711-4	250V RMS, 6 Amp, 7 1/2 ft (2.3 m)	02, 03, 04, 05, 09, 10, 53, 54
B	75778712-2	250V RMS, 10 Amp, 4 ft (1.2 m)	
C	75778703-1	125V RMS, 13 Amp, 4 ft (1.2 m)	
C	75778705-1	125V RMS, 13 Amp, 15 ft (4.5 m)	
D	75778713-0	125V RMS, 10 Amp, 6 ft (1.8 m)	

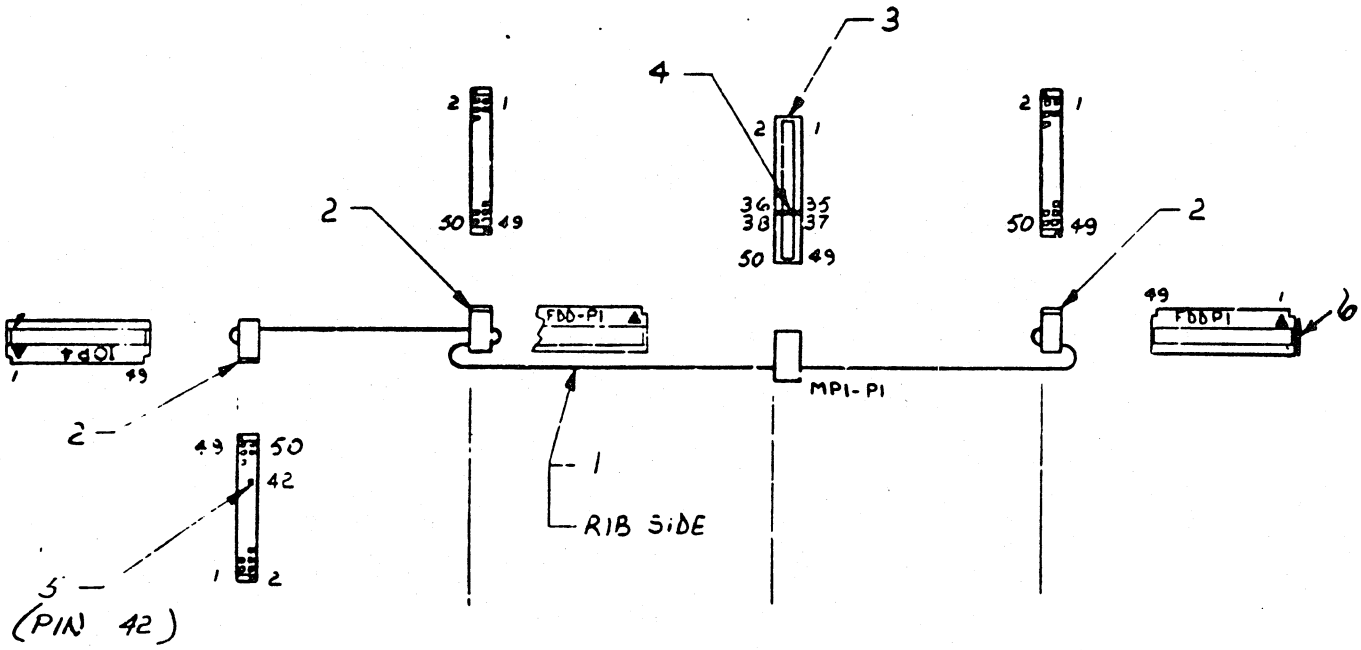
Figure 8-16. AC Power Cord



ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77830724-9	Jumper Plug	220 V, 50 Hz Units
	77830722-3	Jumper Plug	120 V, 60 Hz Units
1	77830710-8	Wire Jumper, Conn. *	
2	77830711-6	Wire Jumper, Conn. *	
3	75724578-2	Connector-Panel Mtg	

* See Figure 3-3 for Jumper Connections for the different input voltage configurations.

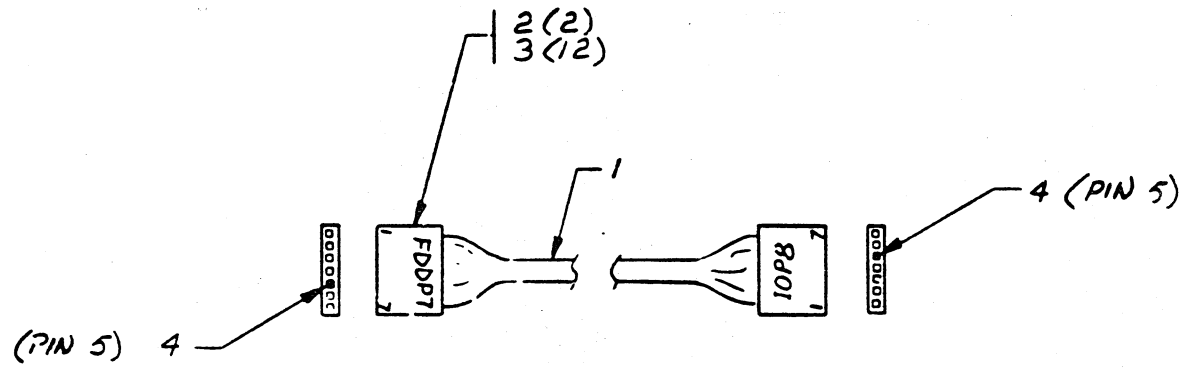
Figure 8-17. Jumper Plug Assembly

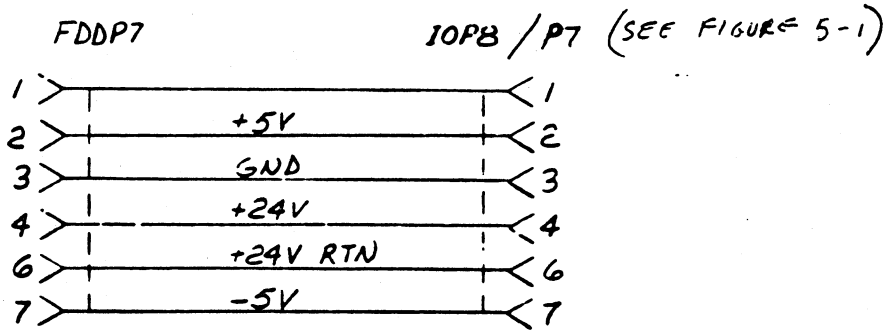


See Figure 5-1 and 5-2 for Signal/Pin Association

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77835240-1	Signal Ribbon Cable-FDD	Used on Master (Fig. 8-6)
	77835241-9	Signal Ribbon Cable-FDD	Used on Slave (Fig. 8-7)
1	65832240-9	Cable-Flat 2.5 in (6.4 mm)	
2	75810305-5	Conn Socket Flat Cab	
3	77830162-2	Connector Flat Cable	77835240 Only
4	77830161-4	Polarizing Key	77835240 Only
5	77830885-8	Polarizing Key	
6	75286253-2	Tape	

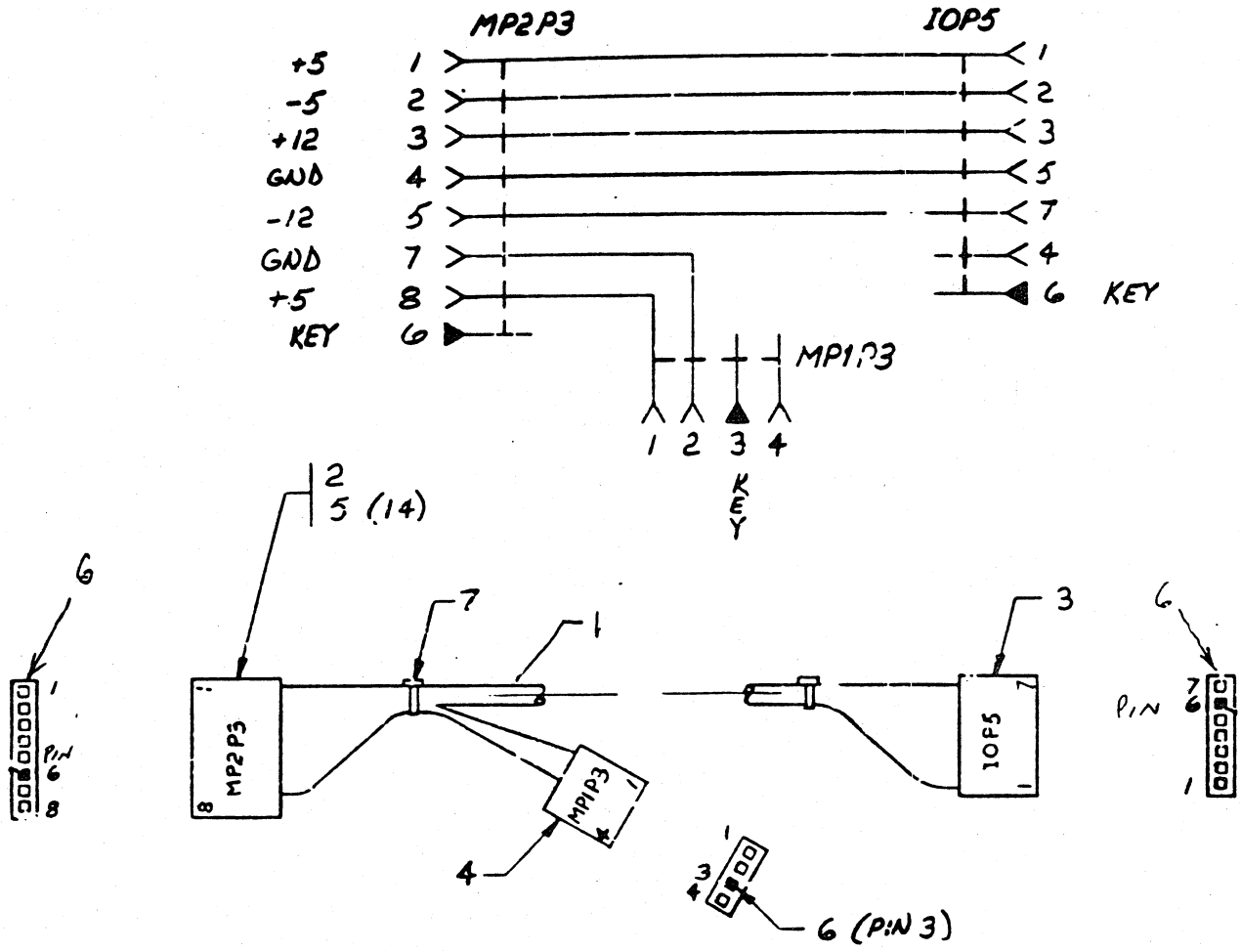
Figure 8-18. Signal Ribbon Cable - FDD/Microprocessor Board





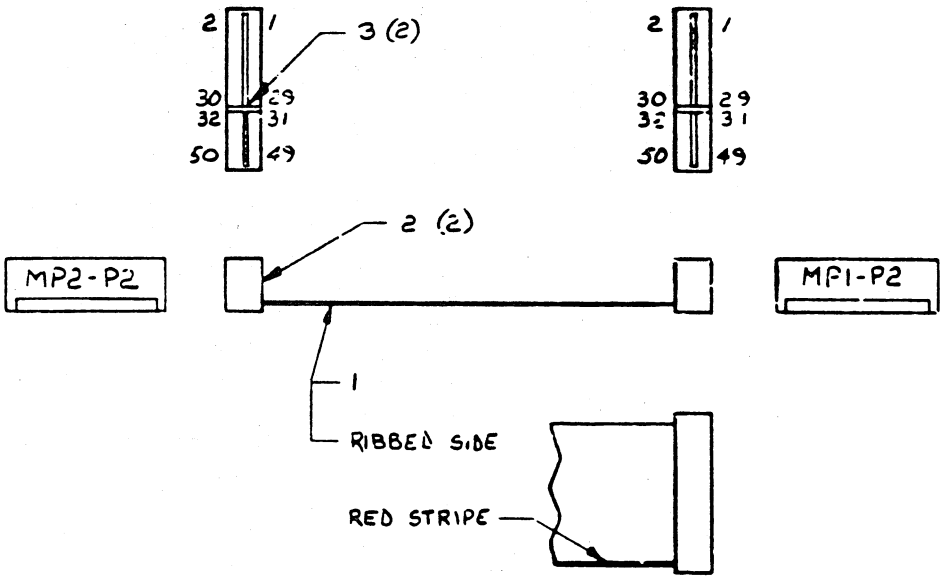
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77835244-3	DC Cable, FDD	I/O PWA to FDD #2 (Fig. 8-6, 8-7)
	77835245-0	DC Cable, FDD	I/O PWA to FDD #1 (Fig. 8-6, 8-7)
1	15003309-0	Wire Elect	
2	77830664-7	Housing	
3	77830663-9	Contact	
4	77830661-3	Keying Plug	
5	94277416-7	Strap, Cable Tie	

Figure 8-19. DC Cable from I/O PWA to FDD Units



ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77835246-8	DC Cable-Logic	See Figure 5-1, 8-11
1	15003309-0	Wire Elect	
2	77830665-4	Housing	
3	77830664-7	Housing	
4	77830666-2	Housing	
5	77830663-9	Contact	
6	77830661-3	Keying Plug	
7	94277416-7	Strap, Cable Tie	

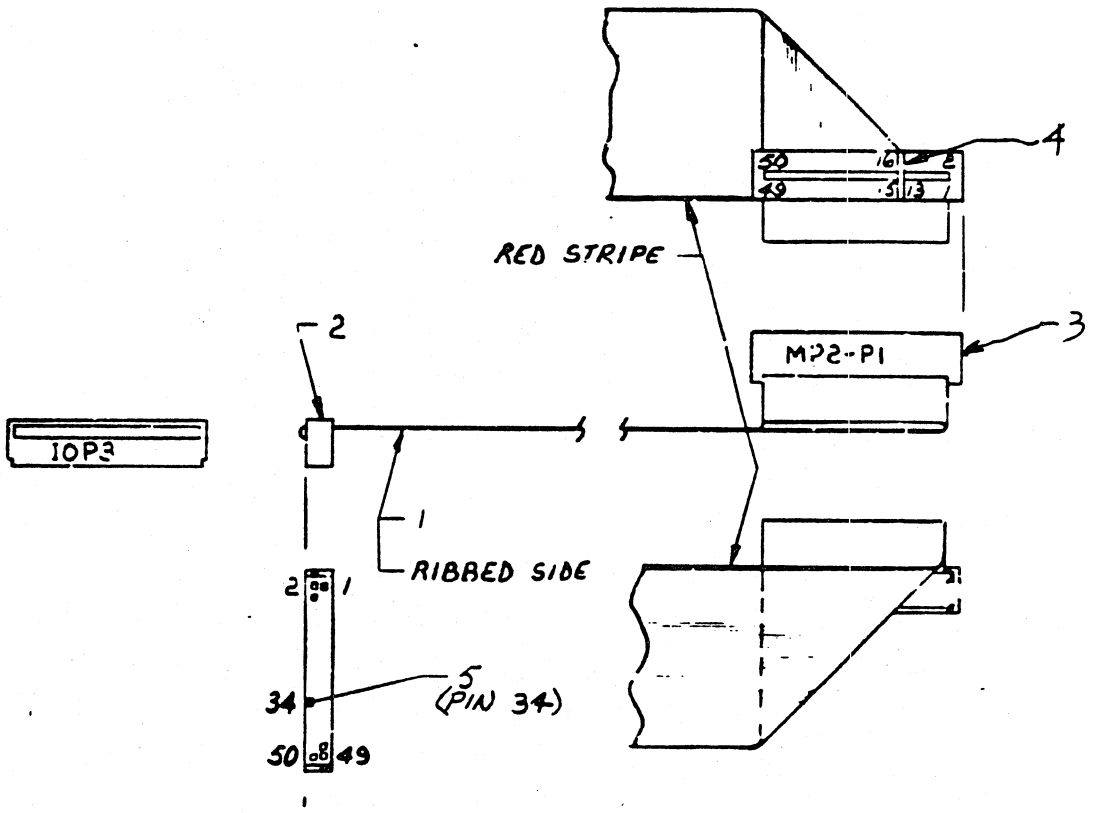
Figure 8-20. DC Cable, I/O PWA to Microprocessor No. 1 to Microprocessor No. 2



Signal/Pin Associations given in Figure 5-1

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77835247-6	Ribbon Cable-Logic Jumper	See Figure 8-11
1	65832240-9	Cable-Flat 2.5 In	
2	77830162-2	Connector Flat Cable	
3	77830161-4	Polarizing Key	

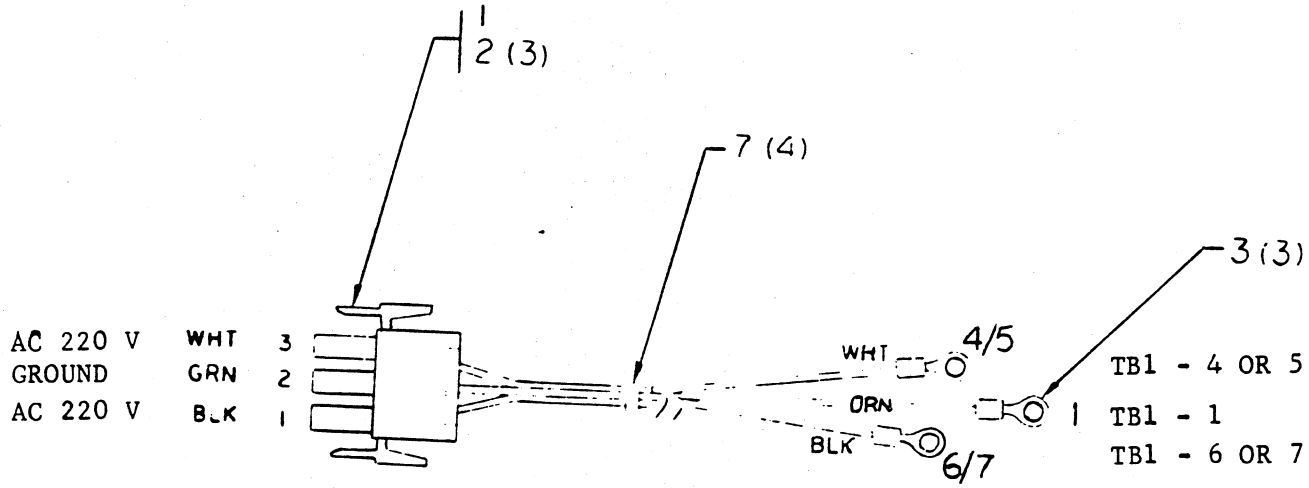
Figure 8-21. Logic Cable - Microprocessor No. 1 to Microprocessor No. 2



Signal/Pin Association given in Figure 5-1

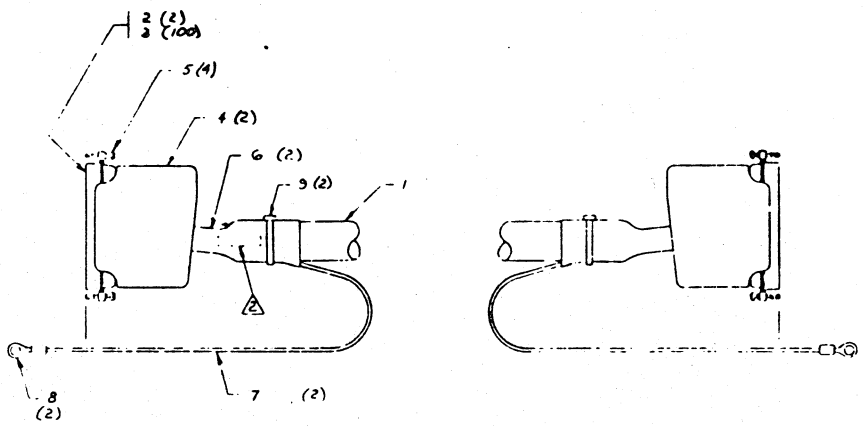
ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77835248-4	Signal Ribbon Cable-Host	See Figures 5-1, 8-15
1	65832240-9	Cable-Flat 2.5 in (63 mm)	
2	75810305-5	Conn Socket Flat Cable	
3	77830162-2	Connector Flat Cable	
4	77830161-4	Polarizing Key	
5	77830885-8	Polarizing Key	

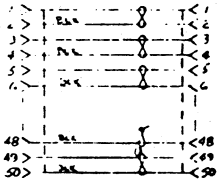
Figure 8-22. Signal Ribbon Cable - Host



ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77832220-6	AC Cable FDD	See Figures 8-6, 8-7
1	83435302-1	Connector, Plug/Cap	
2	83435507-5	Contact	
3	93541016-7	Terminal, Ring Tongue	
4	15003209-2	Wire, White	
5	15003254-8	Wire, Elect 16 Gauge	
6	15003200-1	Wire Elect 16 AWG	
7	94277416-7	Strap, Cable Tie	

Figure 8-23. AC Power Cable to FDD Units from Power Supply

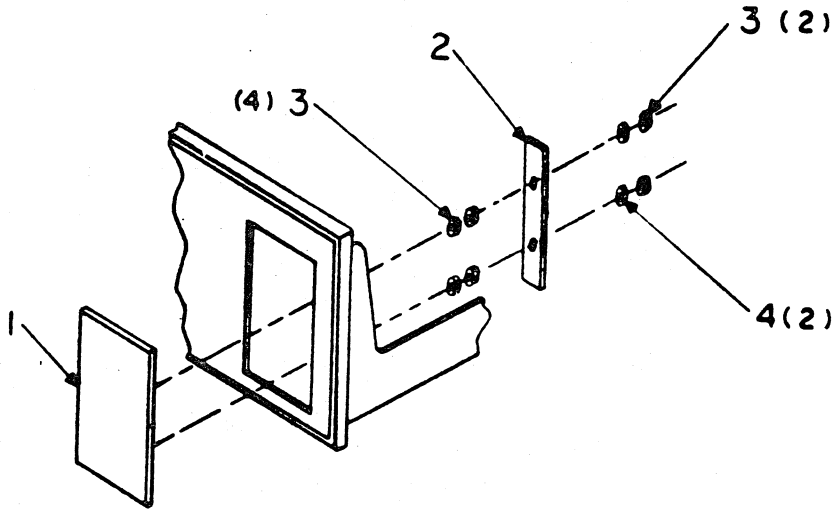




Signal Names given on J-1 of Figure 5-1

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77835249-2	Cable, FDDS Interconnecting	See Figures 3-4, 5-1
1	71022254-2	Cable-Shielded 27 Tp	
2	62013704-2	Connector Pin Housng	
3	62013804-0	Contact Pin	
4	51892204-2	Hood, Connector	
5	18252509-7	Screwlock	
6	24534714-1	Sleeving Heat Shrink	
7	15003354-6	Wire 18 AWG 1061	
8	93541012-6	Terminal, Ring Tongue	
9	94277417-5	Strap-Cable Tie	
10	24534709-1	Sleeving Heat Shrink	

Figure 8-24. FDDS Master to Slave Interconnecting Cable (Optional)



ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
	77834130-5	Dummy Panel Instl Kit	
1	77834900-1	Panel Assembly	
2	77830960-9	Strip	
3	10125105-6	Hex Nut 6-32	
4	10126103-0	Int Tooth Lk Washer	

Figure 8-25. Dummy Panel Installation

APPENDIX A

TYPICAL SEQUENCE/TIMING CHARTS FOR HOST/FDDS INTERFACE

A-1. GENERAL INFORMATION

1. All time units are in microseconds.

2. Two key times are established by the FDDS Subsystem, they are:

   a. Time from FDDS being able to start processing a data enable to the FDDS returning a data strobe (denoted by DS). A maximum of 101 µs may be added to the initial DS time if the FDDS has been idle for four revolutions of the media and is unloading the head.

   b. Time from FDDS returning a data strobe to being able to start processing another data enable (denoted by DE). Notice, that following the rising edge of a data strobe the host can set data enable at any time, however, the FDDS will start processing the data enable only after DE time has elapsed.

3. (H) denotes the time the host delays setting data enable. If host sets data enable prior to the end of previous DE time then (H) = zero.

NOTES

1. The time from point (A) to operation complete interrupt to the host is as follows:

   Single density = (32 x sector length + 348) µs
   Double density = (16 x sector length + 348) µs

2. The time from point (A) to operation complete interrupt to the host is as follows:

   Single density = (32 x sector length + 308) µs
   Double density = (16 x sector length + 260) µs

3. DS = 6 can vary up to 32 µs for single density or 16 µs for double density if the host has caught up with the FDDS reading data from the diskette and storing in the FDDS buffer.

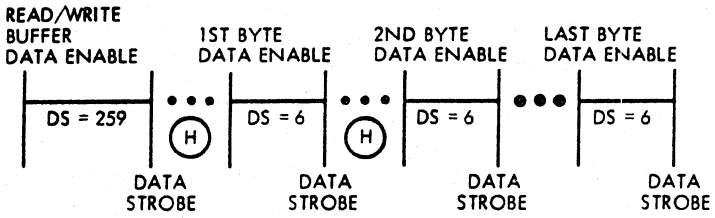
4. DS = 6 can vary up to 32 µs for single density or 16 µs for double density if the host has caught up with the FDDS writing data from the FDDS buffer to the diskette.

5. For consecutive sector writing, (H1) + (H2) + (H3) ≤ 125 µs if the host has transferred the last data byte prior to the operation complete interrupt. If the has not transferred the last data byte, Host Catch-up time + (H1) + (H2) + (H3) ≤ 125 µs.

6. Sector value is automatically incremented by the FDDS.

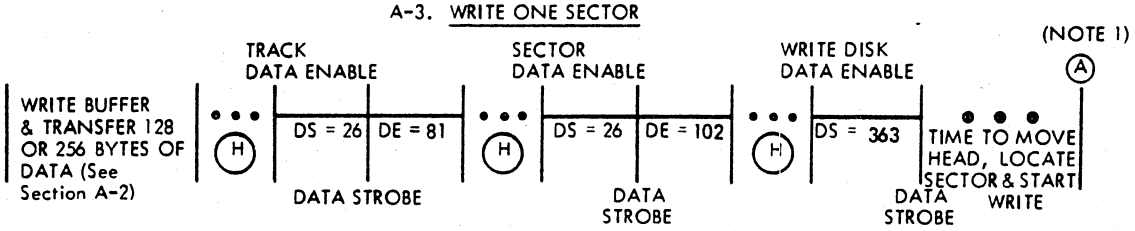
7. For consecutive sector read, (H1) + (H2) + (H3) ≤ 125 µs if the host has transferred the last data byte prior to the operation complete interrupt. If the host has not transferred the last byte, host catch-up time + (H1) + (H2) + (H3) ≤ 125 µs.

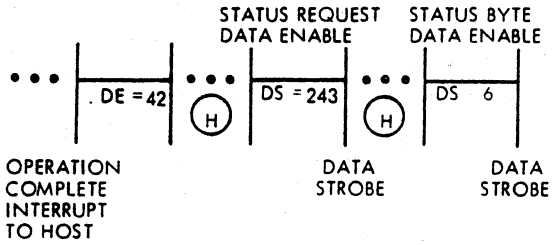
A-2. READ/WRITE BUFFER



BB078a

A-3. WRITE ONE SECTOR

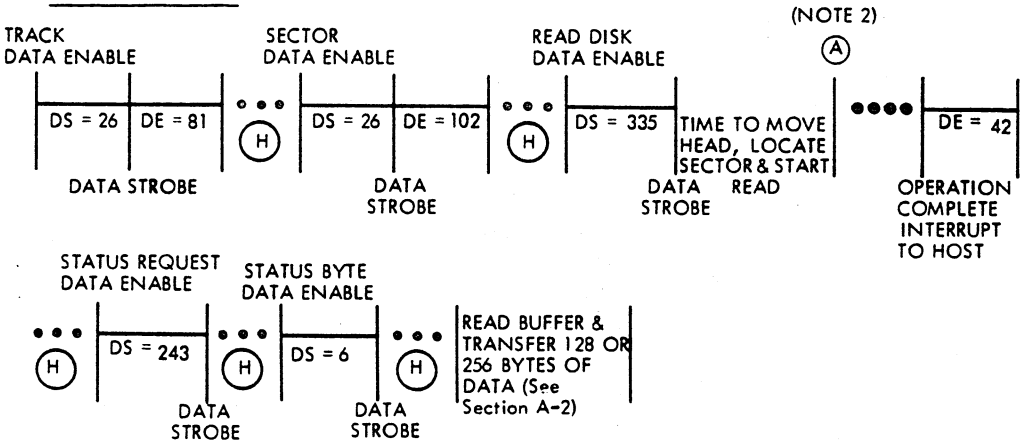




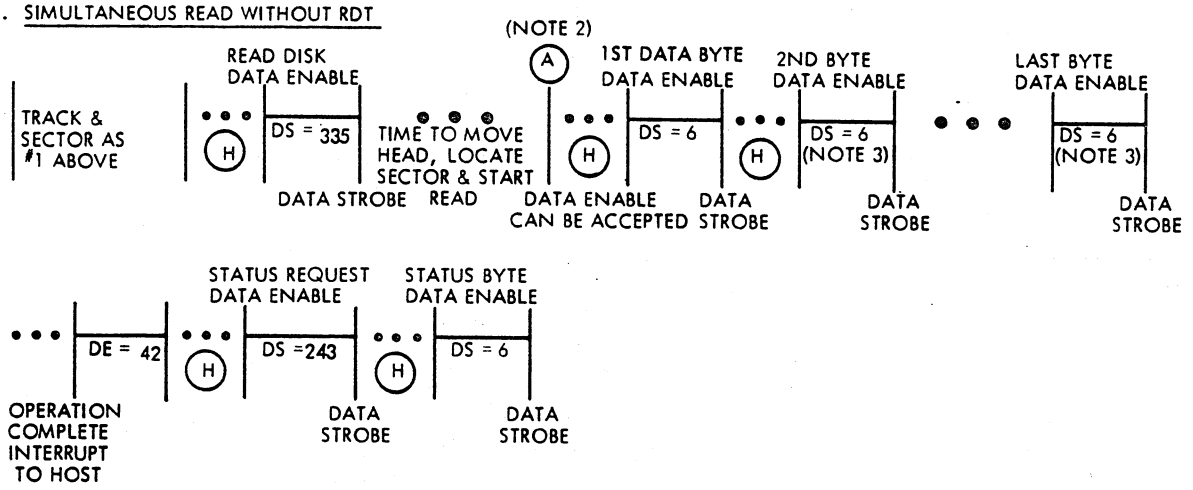
BB078b

A-4. READ ONE SECTOR (3-APPROACHES)

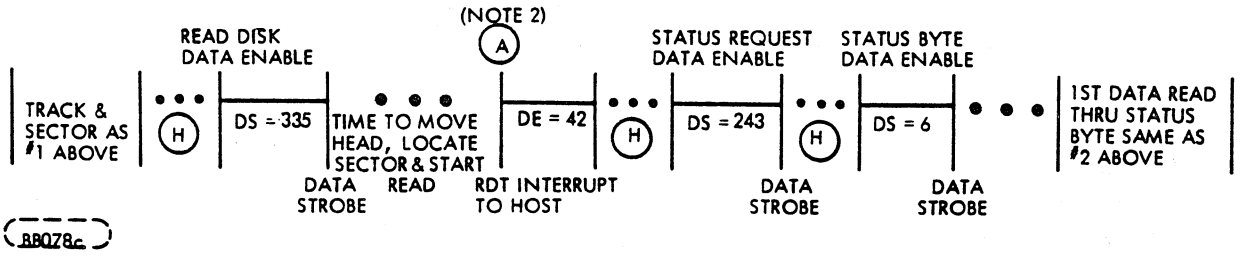
#1. BUFFER OPERATION



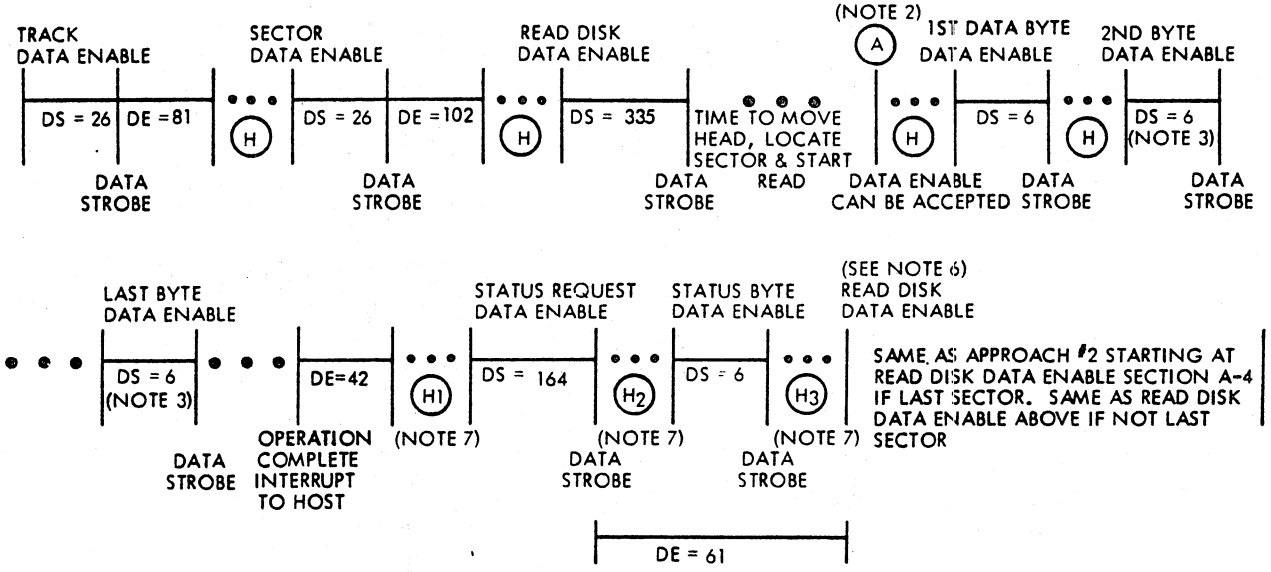
#2. SIMULTANEOUS READ WITHOUT RDT



#3. SIMULTANEOUS READ WITH RDT

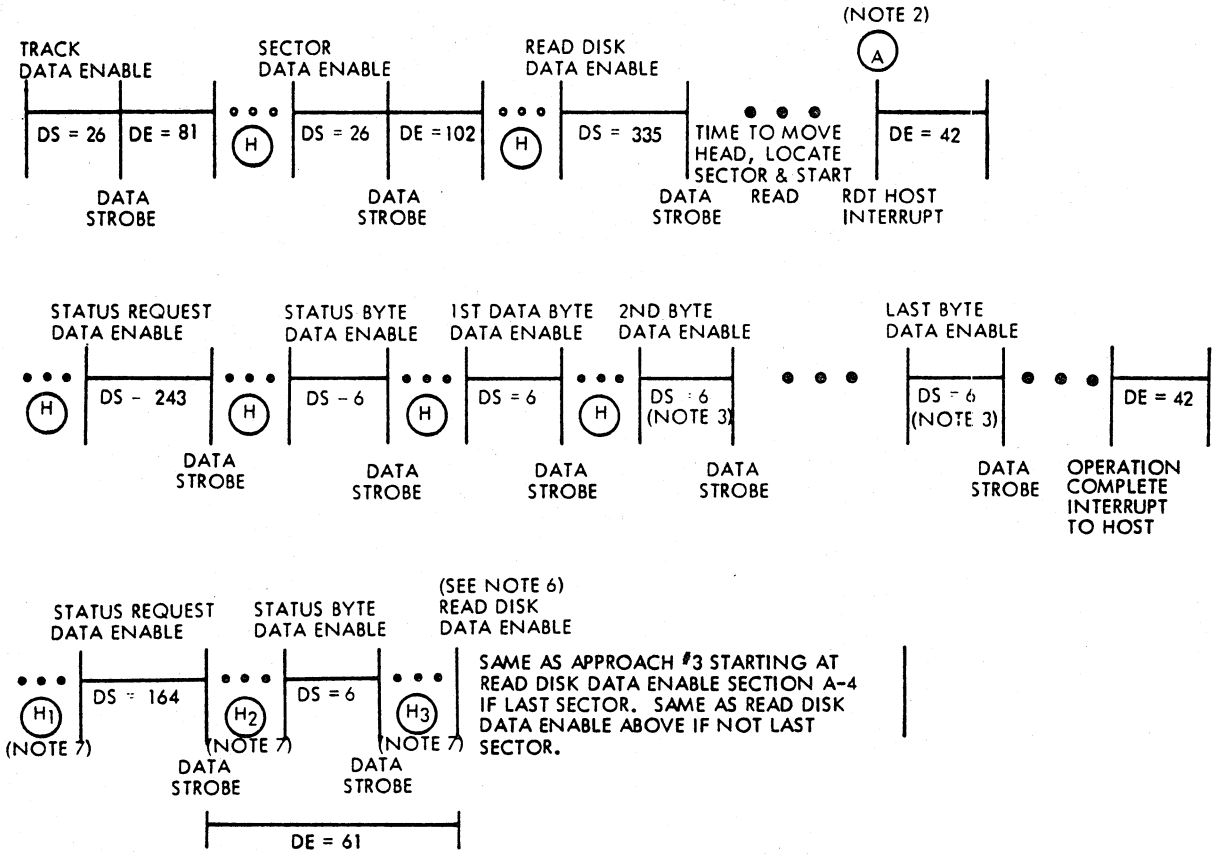


A-7. READ TWO OR MORE CONSECUTIVE SECTORS WITHOUT RDT



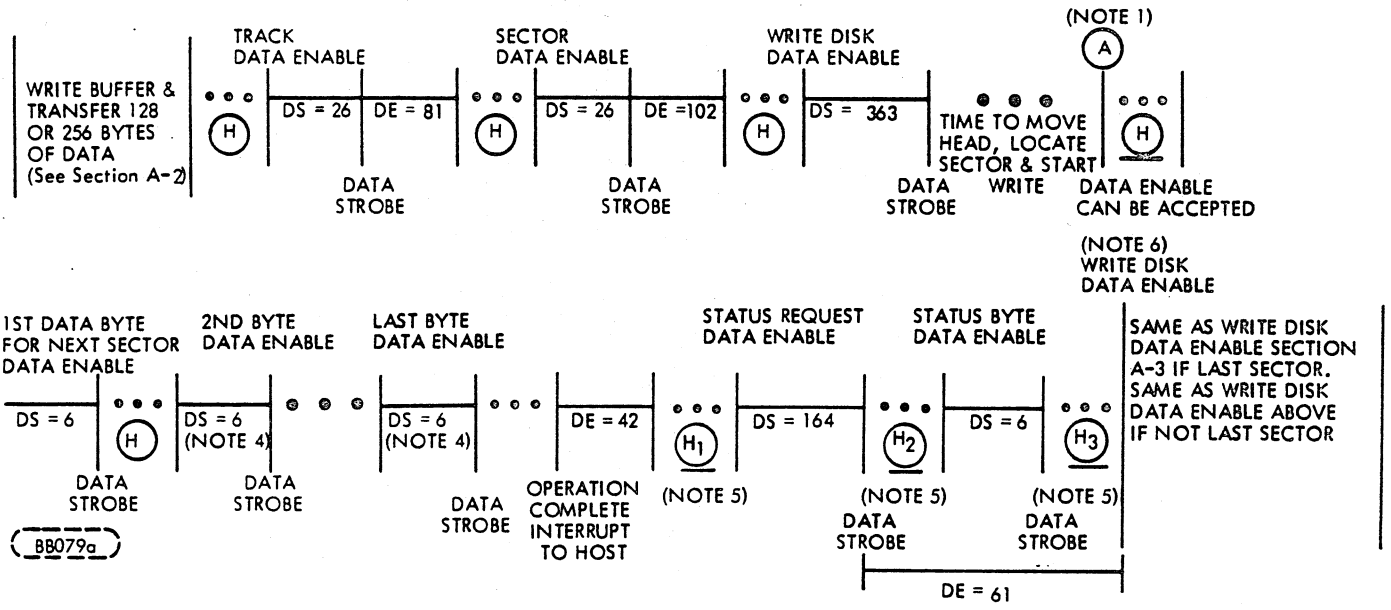
BB080a

A-8. READ TWO OR MORE CONSECUTIVE SECTORS WITH RDT

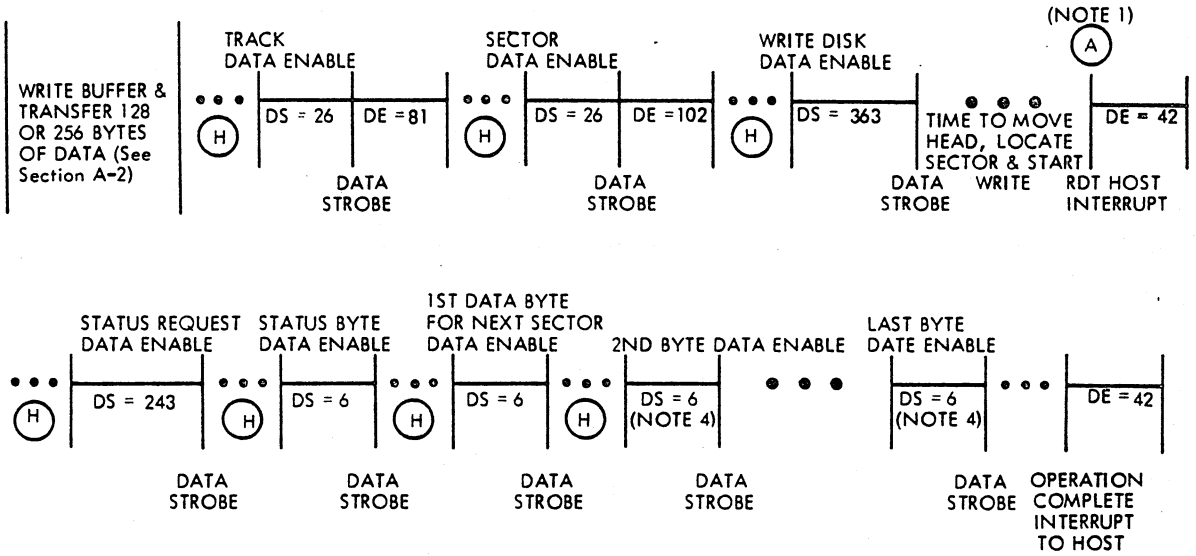


BB080b

A-5. WRITE TWO OR MORE CONSECUTIVE SECTORS WITHOUT RDT



A-6. WRITE TWO OR MORE CONSECUTIVE SECTORS WITH RDT



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